Total No. of Questions : 12] [Total No. of Pages :3

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[3464] - 153
B.E. (E&TC)
COMPUTER NETWORKS
(2003 Course) (404214)

Time : 3 Hours] *[Max. Marks:100*

Instructions to the candidates:

1) *Answer 3 questions from Section I and 3 questions from Section II.*
2) *Answers to the two sections should be written in separate books.*
3) *Neat diagrams must be drawn wherever necessary.*
4) *Figures to the right indicate full marks.*
5) *Use of logarithmic tables, slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.*
6) *Assume suitable data, if necessary.*

SECTION - I

Q1) a) Draw and Explain ISO-OSI reference Model? Comment on Data link control protocols. **[8]**

b) Compare peer to peer networks and client-server networks. **[4]**

c) What is 802.11? Explain Wireless LAN in brief. **[4]**

OR

Q2) a) Explain different service primitives. Compare connection oriented service and connectionless service. **[8]**

b) Explain briefly
   i) Host
   ii) Subnet
   iii) Broadcast network
   iv) Point to Point Network. **[4]**

c) Draw computer network with extended star topology. Explain briefly the advantages and disadvantages of this topology. **[4]**

Q3) a) What is the practical bit rate supported by telephone line? List the different unguided media and explain briefly any one of them. **[8]**

b) Draw and explain functional block diagram of modem. Classify the different protocols used in modem and explain briefly any one of them. **[8]**

P.T.O.

OR

Q4) a) Compare following

i) Circuit switching and Packet switching network

ii) Compare LEO Vs MEO Vs GEO. **[8]**

b) Draw and explain typical cable TV system. How cable video signal and Internet data can be send over the same cable. **[8]**

Q5) a) List the different framing methods and explain any one of them in detail. **[6]**

b) Explain briefly CSMA/CD by taking four nodes as A1, A2, A3 amd A4. Also explain bit map protocol briefly. **[6]**

c) Consider the use of 1000 bit frames on a 1Mbps satellite channel. What is the maximum Links utilization for

i) Stop and wait ARQ.

ii) Continuous ARQ with Window size 7.

iii) Continuous ARQ with Window size 127. **[6]**

OR

Q6) a) Explain the following

i) 1 Persistent CSMA.

ii) Non-Persistent CSMA.

iii) P-Persistent CSMA. **[6]**

b) Compare 802.4 and 802.5 technology. **[6]**

c) A channel has bit rate of 4 kbps and propagation delay is 20 msec. for what range of frame size does stop and wait ARQ technique gives throughput $\geq$ 50%? **[6]**

SECTION - II

Q7) a) How congestion affects network performance. Also explain the difference between flow control and congestion control. **[8]**

b) Explain the Link state routing and its features. **[4]**

c) Compare virtual circuit and datagram networks. **[4]**

OR

Q8) a) Explain the different QoS parameters. Also write about transport service primitives. **[8]**

b) Explain connection establishment and connection termination with respect to the transport layer. **[4]**

c) Explain token Bucket algorithm briefly. **[4]**

Q9) a) Explain DES algorithm in detail. **[8]**

b) How electronic mail system work? What is the role of SMTP and POP-3 server in this E-mail System? **[8]**

OR

Q10)a) Write a short note on "Video on Demand". **[8]**

b) What is Socket? What are socket primitives? What will be the socket address of machine having IP address = 192.168.3.101 in case of webserver (http) and FTP server installed on the same machine. **[8]**

Q11)a) Explain "X" Windows system in TCP/IP. **[6]**

b) Explain Telnet server and Telnet client communication. Can you use Telnet for LAN as well as Internet? **[6]**

c) Compare TCP and UDP. **[6]**

OR

Q12)a) Explain the TFTP and BOOTP in TCP/IP communication. **[6]**

b) Explain Traceroute utility with respect to TCP/IP. **[6]**

c) Explain the ARP and RARP protocols operation in LAN. **[6]**

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[3464] - 154
B.E. (E&TC)
VOICE NETWORKS
(2003 Course)

Time : 3 Hours] *[Max. Marks:100*

Instructions to the candidates:

1) *Answer 3 questions from Section I and 3 questions from Section II.*
2) *Answers to the two sections should be written in separate books.*
3) *Neat diagrams must be drawn wherever necessary.*
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5) *Assume suitable data, if necessary.*

SECTION - I

Q1) a) Explain the block diagram of Distributed SPC organization. **[8]**

b) Derive the expression for Unavailability of Single and Dual processor configuration. Given that MTBF = 3000 hrs and MTTR = 6 hrs, calculate the availability and Unavailability of Single and Dual processor system. The life of exchange is 20 yrs. **[10]**

OR

Q2) a) Describe the working of Input controlled Time division space switch? An analog non-folded time division space switch is to be designed to support 32 inlets and outlets each. Assuming bi-directional traffic calculate:

i) The time duration for exchanging samples for one connection.

ii) Size of control memory if switch is output controlled.

iii) Clock rate. **[10]**

b) Explain the design consideration of DTMF dialler. **[8]**

Q3) a) Differentiate between Loss system and Delay system. Explain Lost Call Cleared model in traffic Engineering. **[8]**

b) The traffic statistics of a company using a EPABX indicates that 200 outgoing calls are initiated every hour during working hours. Equal number of calls comes in. Each call lasts for 180 seconds on the average. If the G.O.S required is 0.07, determine the no. of lines required between the EPABX and main exchange. **[8]**

P.T.O.

OR

Q4) a) Derive the expression for Poisson's arrival process and its significance. **[8]**

b) Following data was recorded by observing the activity of a single customer line during the eight hour period from 7.00 a.m to 3.00 p.m. Determine the traffic intensity during the eight hour period during the busy hour from 10.00 a.m to 11.00 a.m.

Call No.	Call Started	Call Terminated
1	7:10	7:15
2	8:25	8:28
3	9:45	9:52
4	10:01	10:09
5	10:22	10:27
6	10:35	10:43
7	11:18	11:26
8	1:04	1:11
9	2:20	2:29

[8]

Q5) a) Compare N-ISDN with B-ISDN. List the benefits and services of ISDN. **[8]**

b) Describe in detail the architecture of the frame relay network. **[8]**

OR

Q6) a) Explain in detail the architecture of ISDN and its objectives. **[8]**

b) Compare BRI and PRI architecture of ISDN. **[8]**

SECTION - II

Q7) a) Explain in detail the terms:

i) Spectral efficiency

ii) Frequency Reuse

iii) Cell splitting

iv) Cell sectorization **[12]**

b) Explain different interference reducing mechanism in GSM. **[6]**

OR

Q8) a) Explain with the flow diagram a step by step process for outgoing call setup in GSM network. **[8]**

b) Explain with block diagram the GSM architecture and its evolution. **[10]**

Q9) a) Define Handover. Explain in detail following Hand-off mechanisms in CDMA.

i) Intersector Handoff

ii) Intercell Handoff

iii) Soft-Softer Handoff

iv) Hard Handoff. **[8]**

b) Describe the flow diagram to grant traffic channel in CDMA. **[8]**

OR

*Q10)*a) Compare GSM & IS-95 CDMA architecture w.r.t following parameters:

i) Frequency Band ii) Channel Bandwidth

iii) Voice Quality iv) Interference

v) Handoff vi) System capacity

vii) Radio interface viii) Economics **[8]**

b) Explain various registration supported by IS-95 architecture. **[8]**

*Q11)*a) Describe in detail Interexchange signaling in VoIP. **[8]**

b) Explain the architecture of Session Initiation Protocol and call signaling between two user agents. **[8]**

OR

*Q12)*a) Define VoIP? Draw and explain the various elements of Voice over IP network. **[8]**

b) Describe in detail Media Gateway control Protocol. **[8]**

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[3464]-155
B.E. (E & TC)
ELECTRONIC PRODUCT DESIGN
(2003 Course)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Use of electronic pocket calculator is allowed.***
6) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explain role of line filters, movs, Tranzorbs and suppressor capacitor in hardening of power supply against line voltages. [8]

b) Compare quiescent power consumption of LS TTL and HC-CMOS devices for frequencies below and above power cross over frequency. Justify your answer. [6]

c) A CMOS gate is feeding load capacitance C_L = 100 PF at frequency 1 MHz. If V_{CC} = 6 volts, find power consumption due to charging and discharging of C_L. [4]

OR

Q2) a) With the help of practical example establish techno commercial feasibility of an electronic product. [8]

b) Draw symbols of safety ground, signal ground and return ground. Also give typical application of each. [6]

c) A power supply system is designed with one transformer, four rectifier diodes, 3 capacitors & one regulator IC with failure rates 0.6, 0.2, 0.3 and 0.18 per 10^6 hours respectively. Find reliability of a system after 2×10^6 hours. [4]

Q3) a) What is ground bounce. Explain the recommended PCB design practices to reduce ground bounce in high speed circuits. [8]

b) Calculate the parasitic elements for following PCBs.

i) Resistance of 10 cm long copper track with 0.8 mm width on 35 μm Cu clad laminate with resistivity of Cu = $1.72 \times 10^{-6} \Omega$ - cm.

ii) Capacitance of two 1.5mm wide tracks on opposite faces of a double sided PCB each with track length 20 cm, laminate thickness is 1.6 mm and relative permittivity is 4.2 [8]

OR

Q4) a) Explain the different termination schemes for avoiding reflections in high speed circuits. [4]

b) Why different logic family signal traces should not be mixed together. [4]

c) Explain recommended PCB design practices for i) Power supply and ground routing ii) decoupling. [8]

Q5) Explain with justification and schematic arrangement the type of instrument you will use to find faults in following: [16]

a) Setup/hold timing violations in microcontroller circuit.

b) Verification of all inputs and outputs of ADC.

c) Measure turn off time of IGBT.

d) Embedded software execution to be tested.

OR

Q6) a) What is signal integrity. How it can be assured for high speed circuits. [8]

b) With suitable practical example explain the use and limitations of operating point analysis and ac analysis. [8]

SECTION - II

Q7) Write short notes on: [16]

a) Structured programming.

b) Steps in programming assembly code on PC.

c) Standard methods of debugging software.

d) Real time software.

OR

Q8) A volting machine is to be designed using ASM. Consider full automatic operation and also draw ASM chart for the same. [16]

Q9) a) What are sources of EMI. How it is regulated using filters. [8]

b) What are different vibration tests to be carried out on an industrial product. Also indicate different parameters associated with this test. [8]

OR

Q10) a) Specify with justification the choice of environmental tests to be carried out on following products: [8]

i) Palmtop

ii) MRI machine

iii) Washing machine

b) What is importance of temperature cycling test and dry heat test for medical equipments. What are important parameters for these tests. [8]

Q11) Take an example of suitable electronic product and draw/prepare foliowing documents. [18]

a) PCB fabrication drawing.

b) Wiring diagram.

c) Bill of material

d) Product test specifications.

OR

Q12) Give reasons: [18]

a) Multilayer PCBs must be used for ICs packaged as PLCC.

b) A good service manual gives fault tree.

c) Paper phenolic laminates are not suitable for industrial products.

d) Types of documents required, their use and formats.

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[3464] - 156
B.E. (E&TC)
VLSI DESIGN
(2003 Course) (404217)

Time : 3 Hours] *[Max. Marks:100*

Instructions to the candidates:

1) ***Answer 3 questions from Section I and 3 questions from Section II.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Differentiate std-logic and std-ulogic with example? **[4]**

b) Explain with example: delays in VHDL. **[5]**

c) What is significance of following terms in VHDL

i) Library ii) Use iii) Invisible library. **[9]**

OR

Q2) a) Write VHDL code and test bench for 2 input Ex -NOR gate design with minimum number of 2 input NAND (s) only as a component using structural modelling. **[9]**

b) Write VHDL code and test bench to perform tabulated operations for mode 'M' and output Y and Z. Where A is 3-bit input data. **[9]**

M	Function F (Y, Z)
0	$Y = A^2 - 8$
1	$Z = A^2 + 16$

Q3) a) Explain the term 'Metastability' with example. **[4]**

b) Draw FSM for **[12]**

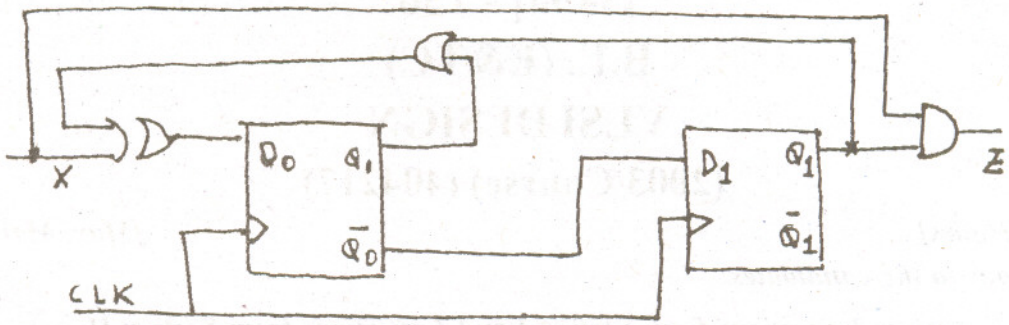
i) T–Flip Flop.

ii) S–R Flip Flop and write VHDL code. Also write test bench which will cover all state table conditions.

OR

P.T.O.

Q4) For following RTL shown in fig (4–a) design FSM & write VHDL code & test bench. **[16]**



(Fig 4-a)

Where X and Z are input and outputs of a system respectively.

Q5) a) Differentiate SRAM Vs Antifusable FPGA? **[8]**

b) Explain selection criteria for CPLD design? **[8]**

OR

Q6) a) Explain antifusable FPGA architecture? **[8]**

b) Differentiate CPLD, FPGA & ASIC? **[8]**

SECTION - II

Q7) a) Write short notes on **[9]**

i) SRC

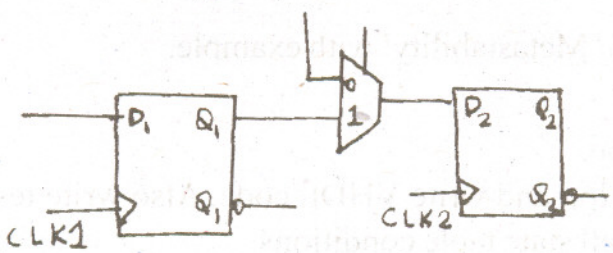
ii) DRC

iii) Power optimization.

b) Explain with waveform that how much clock skew between CLK1 and CLK2 can be tolerated in following circuits in fig (7 - b) when **[9]**

i) CLK 1 is delayed after CLK 2

ii) CLK 2 is delayed after CLK 1



(Fig 7-b)

OR

Q8) a) Write short notes on **[9]**

i) Design validation.

ii) EMI immune design.

iii) Off chip connections.

b) Draw circuit diagram, waveform and explain the operation of 6T SRAM cell. **[9]**

Q9) a) Explain with neat legends for n-well CMOS layout design rules with respect to i) Maximum size & ii) Minimum size spacing for: 1) n-well 2) poly 3) metal 4) active area. **[8]**

b) Explain static & dynamic power dissipation. Derive an expression for power delay product. **[8]**

OR

*Q10)*a) Why NAND is prefered over NOR gate? Draw 4 :1 multiplexer using transmission gate. **[8]**

b) Design CMOS logic gates for $Y = \overline{A\,B + C\,(D+E)}$. Calculate area needed on the chip. **[8]**

*Q11)*a) What is IEEE standard for boundary scan? Explain boundary scan architecture. **[8]**

b) What do you mean by design for testability? How it can be categorized? Where it is useful? **[8]**

OR

*Q12)*a) Differentiate **[8]**

i) Testing Vs Verification.

ii) White box Vs Black box testing.

b) Explain why model faults? Explain different fault models with schematics? **[8]**

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[3464] - 160
B.E. (E & T/C)
ARTIFICIAL NEURAL NETWORKS
(2003 Course)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:-

1) *Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10, Q11 or Q12.*
2) *Answers to the two sections should be written in separate books.*
3) *Neat diagrams must be drawn wherever necessary.*
4) *Figures to the right indicates full marks.*
5) *Use of electronic pocket calculator is allowed.*
6) *Assume suitable data, if necessary.*

SECTION - I

Q1) a) What are the main differences among the three models of artificial neuron namely McCulloch-Pitts, Perceptron and adaline? **[5]**

b) Compare the performance of artificial neural network with that of biological neural network. **[5]**

c) Explain the following learning laws: **[3]**

i) Instar learning law.

ii) Outstar learning law.

d) Compare supervised learning and unsupervised learning. **[3]**

OR

Q2) a) What are the different types of Hebbian learning? **[4]**

b) What are the different types of competitive learning? **[4]**

c) Explain the distinction between stability and convergence. **[4]**

d) Explain the following:

i) Additive and shunting models of activation models. **[4]**

Q3) a) Explain the difference between single layer perceptron and multilayer perceptron. **[2]**

b) Draw the architecture of adaline and explain the training algorithm used in adaline. **[8]**

c) Given 2 input neuron with the following parameters, bias b = 1.2, weight matrix W = [3 2] and input I = [-5 4]. Calculate the neuron output for the following transfer function: **[6]**

i) Symmetrical hard limit function.

ii) Saturating linear function.

iii) Log sigmoid function.

OR

Q4) a) Explain the architecture of backpropagation network and the training algorithm used in backpropagation network. **[7]**

b) Explain what do you mean by backpropagation with momentum? **[3]**

c) Explain the difference between Madaline rule I (MR I) and Madaline rule II (MR II) algorithms. **[4]**

d) What are the initial weights and bias assumed in MR I training algorithm between the hidden and output units? Can they be varied? **[2]**

Q5) a) What is feedback network? **[3]**

b) What are pattern storage networks? **[3]**

c) What is state transition diagram for a feedback network? Explain how to derive it for a given network. **[12]**

OR

Q6) a) What is meant by simulated annealing? What is annealing schedule? **[6]**

b) Describe the architecture of Boltzmann machine. **[4]**

c) Explain the learning algorithm used in Boltzmann machine. **[5]**

d) What do you mean by the term storage capacity? **[1]**

e) Define energy function in Hopfield network. **[2]**

SECTION - II

Q7) a) What is simple competitive learning? Explain the training algorithm used in simple competitive learning. **[6]**

b) Explain the architecture of Maxnet with the help of neat diagram and explain how it can be used as a subnet. **[6]**

c) Explain Learning Vector Quantization (LVQ). **[4]**

OR

Q8) a) Explain in detail the principal component analysis networks. **[5]**

b) What is stability plasticity dilemma? **[3]**

c) Explain the architecture of ART 1 network and training algorithm used in ART 1 network. **[8]**

Q9) a) Explain the difference between auto associative and hetero associative networks. **[4]**

b) What is bidirectional associative memory (BAM)? Explain how training and testing is performed in BAM with the help of an example. **[8]**

c) What are the requirements of an associative memory? **[4]**

OR

*Q10)*a) Explain Multidirectional associative memory (MAM). Explain why MAM will have superior performance over BAM for pattern retrieval. **[6]**

b) Explain the distinction between pattern association and pattern classification. **[4]**

c) Explain the architecture of RBF networks. Explain how they can be used for function approximation. **[6]**

*Q11)*a) What is a local minima problem in optimization and how is mean field annealing applied in the solution of optimization problem? **[6]**

b) Explain how neural network approaches are useful for a texture classification problem. **[6]**

c) Explain how image smoothing problem can be solved with the help of neural networks. **[6]**

OR

*Q12)*a) What is a convolutional network architecture and how is it useful for the problem of handwritten digit recognition? **[6]**

b) What are some direct applications of the principles of neural networks? Why are they called 'direct applications'? **[6]**

c) Explain the difficulties in the solution of travelling salesman problem by a feedback neural network. **[6]**