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[3664]-214

B.E. (Electronics)

VLSI DESIGN Sem - I

(New 2003 Course)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates :

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Use of logarithmic tables, slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.***
6) ***Assume suitable data, if necessary.***

SECTION - I

Q1) Write VHDL Code for mux 8 : 1 using any two modelings and also write test bench for it. **[16]**

OR

Q2) a) Explain VLSI Design Flow. **[8]**

b) Write VHDL Code for Decoder 2 : 4. **[8]**

Q3) Draw SM chart and write VHDL code for VART Transmitter. **[16]**

OR

Q4) By considering suitable examples, explain different techniques of state minimization. **[16]**

Q5) Draw block diagram and explain detail architecture of CPLD. **[18]**

OR

Q6) Draw block diagram and explain detail architecture of FPGA. **[18]**

P.T.O.

SECTION - II

Q7) Explain different types of memory. **[16]**

OR

Q8) Explain different types of power distribution and optimization techniques is CMOS VLSI circuits. **[16]**

Q9) What is Scaling, what are different scaling parameters? Explain constant field and constant voltage scaling. **[16]**

OR

Q10) With respective VTC explain the operation of CMOS Inverter. Also derive for CMOS Inverter. **[16]**

$[W/L]_P = 2\ [W/L]_N$

Q11) a) What is fault coverage, explain with examples different stuck faults. **[9]**

b) Explain with block diagram full and partial scan. **[9]**

OR

Q12) Write short notes on : **[18]**

a) TAP controller.

b) DFT.

c) BIST

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