Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

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S.E. (Computer Engg.) (I Sem.) EXAMINATION, 2009

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2003 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer questions **1** or **2**, **3** or **4**, **5** or **6** from Section I and questions **7** or **8**, **9** or **10**, **11** or **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) What will be the gray code of any given 4-bit binary number ? Show the truth table. [6]

(*b*) Perform the following Hexadecimal subtractions using 2's complement method : [6]

(*i*) $(42)_{Hex} - (28)_{Decimal}$

(*ii*) $(2A)_{Hex} - (78)_{Decimal}$.

(*c*) Explain the following numbers in decimal. Show step-by-step solutions and calculation : [6]

(*i*) $(1010.010)_{Binary}$

(*ii*) $(57A.2C)_{Hex}$.

P.T.O.

Or

2. (*a*) How to convert any 4-digit Hex number into equivalent 4-digit decimal number ? Write steps. Also solve the following to find equivalent decimal : [8]

(*i*) $(3A8)_{Hex}$

(*ii*) $(59C)_{Hex}$.

(*b*) Apply Boolean algebra and minimize the following functions. Also draw equivalent ckt. diagram using basic logic gates : [10]

(*i*) $A\bar{B}\bar{C} + A\bar{B}C + \bar{A}B + A\bar{C} + BC$

(*ii*) $(A + \bar{B} + C) . (A + \bar{C}) . (\bar{B} + C) . (B + \bar{C})$.

3. (*a*) Draw the 2-i/p standard TTL NAND gate circuit and explain its operation with truth table. [8]

(*b*) Explain various properties of TTL logic family. Comment on fan-in and fan-out. [8]

Or

4. (*a*) Compare TTL and CMOS logic family. Also draw NOR-CMOS logic gate. [8]

(*b*) Give classification of logic family in detail. [8]

5. (*a*) Draw and explain 4-bit BCD adder using 7483. Explain the working with example. [8]

(*b*) Design 14 : 1 mux using 4 : 1 mux (with enable inputs). Explain the working of ckt in brief. [8]

Or

6. (*a*) Solve using Quine-McClusky method and determine prime implicants for $z = f(A, B, C, D) = \Sigma(0, 1, 3, 8, 10, 12)$. [8]

(*b*) Explain in brief the design of Grey-code to excess-3 code conversion. Show k-map and circuit diagram of your design. [8]

SECTION II

7. (*a*) What is MOD counter ? Design MOD-33 counter using IC 74 90. Explain your design. [12]

(*b*) What is lock-out condition ? How to avoid it ? [6]

Or

8. (*a*) Draw and explain types of shift register. Explain any *one* application of such register. [10]

(*b*) What is MS-J-K Flip-Flop ? Explain the advantage of such Flip-Flop. Draw suitable circuit diagram and timing diagram. [8]

9. (*a*) Explain Entity-Architecture of VHDL. Explain the same for 2-i/p NOR gate. [8]

(*b*) Explain ASM chart in brief. [4]

(*c*) Explain RTL design steps in brief. [4]

Or

10. A sequential ring counter circuit with present state '010'. The circuit also have an input 'X'. If X = 0 then circuit will show next output (UP COUNT) else for X = 1, it goes to '010' state. Draw ASM chart with all possible status. [16]

11. (*a*) What is PLD ? What is the difference between PAL and PLA ? Explain with the help of neat diagram. [8]

(*b*) Draw and explain structural diagram of CPLD and FPGA. Also explain the difference between these two types of devices. [8]

Or

12. (*a*) Explain in detail the architecture of CPLD. How will you program CPLD ? Do you know any tool to design such devices ? Explain various design steps of circuits using CPLD. [10]

(*b*) Implement 4 : 1 mux using suitable PAL. [6]