Total No. of Questions—**12**] [Total No. of Printed Pages—**4+1**

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S.E. (Computer Engg.) (I Sem.) EXAMINATION, 2009

ELECTRONICS DEVICES AND CIRCUITS

(2003 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer Question Nos. **1** *or* **2**, **3** *or* **4** and **5** *or* **6** from Section I and Question Nos. **7** *or* **8**, **9** *or* **10** and **11** *or* **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Explain : [8]

(*i*) Thermistor bias compensation

(*ii*) Diode bias compensation.

(*b*) State *three* stability factors S, S', S" for biasing circuits and derive equations of S, S' and S" for self bias circuit. [10]

Or

2. (*a*) Compare fixed bias, collector to base bias and self bias circuits with respect to : [8]

(*i*) Circuit diagram

(*ii*) Biasing resistances and its location

(*iii*) Pretence of negative feedback

(*iv*) Equation for stability factors.

P.T.O.

(*b*) A silicon transistor operated with self bias gives V_{CEQ} = 5 V, I_{CQ} = 2 mA for V_{CC} = 10 V and R_C = 2 kΩ. If β for transistor is 50, V_{BE} = 0.7 V and stability factor S is 5, calculate the values of biasing resistors R_1, R_2 and R_E. [10]

3. (*a*) Draw the hybrid model for typical common emitter amplifier without R_E and derive expression for A_i, R_i, A_v and R_o. [10]

(*b*) Write a short note on Bootstrapped emitter follower. [6]

Or

4. (*a*) A common base amplifier, as shown in Fig. 1 has the following components :

R_S = 600 Ω, R_C = 5.6 kΩ, R_E = 5.6 kΩ, R_L = 39 kΩ. The transistor parameters are h_{ie} = 85 and h_{oe} = 2 μA/V. Calculate R'_i, R'_o, A_v and $A_{vs} = V_o/V_s$. [10]

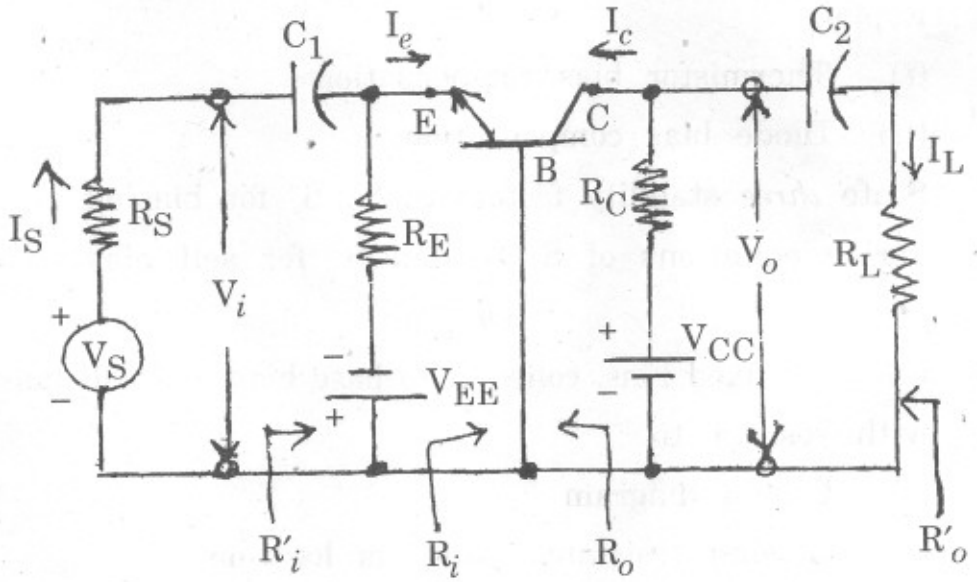

Fig. 1

(*b*) Write a short note on Miller's theorem. [6]

5. (*a*) An ideal class B complementary symmetry push-pull amplifier operates with V_{CC} = 12 V and R_L = 5. If input is sinusoidal, calculate : [10]

(*i*) Maximum power output

(*ii*) Power dissipation in both transistor

(*iii*) Power dissipation in each transistor

(*iv*) Conversion efficiency for maximum power output.

(*b*) Explain various types of coupling in multistage amplifiers. [6]

Or

6. (*a*) For the circuit shown in Fig. 2, assume both transistors to be identical with h_{ie} = 1.1 kΩ, h_{fe} = 50 and negligible h_{re} and h_{oe}. Calculate R_i, R_o, A_v and A_{vs}. [10]

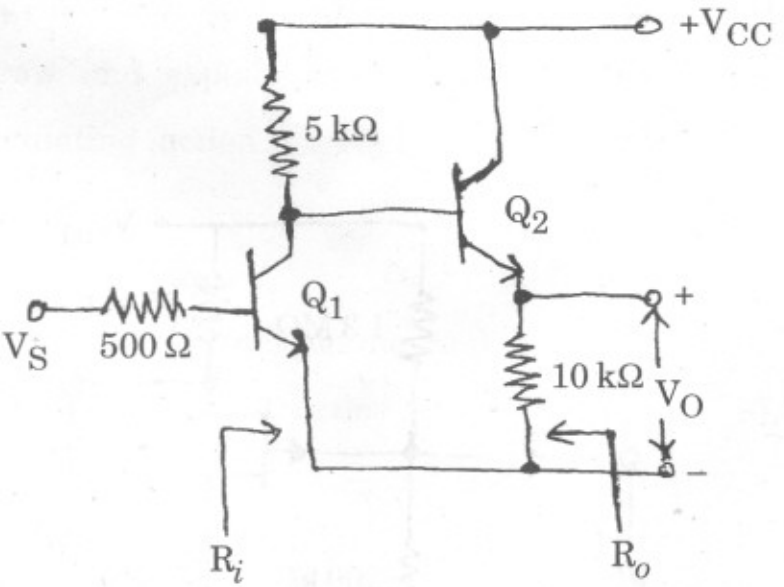

Fig. 2

(*b*) Explain harmonic and cross over distortion in large signal amplifiers. [6]

SECTION II

7. (*a*) A *p*-channel FET has an I_{DSS} = –12 mA, V_P = 5 V, V_{GS} is 5.32 V. Calculate drain current, transconductance. [8]

(*b*) With the help of neat diagram, explain the operation of *n*-channel JFET. Show the internal depletion regions and explain their shape. Also draw static o/p characteristic of JFET. [10]

Or

8. (*a*) What do you understand by 'pinch off voltages' and 'cut-off voltages' in JFET ? Draw and explain transfer characteristics of JFET. [8]

(*b*) For the circuit shown in Fig. 3, *p*-channel JFET has V_P = 4 V, I_{DSS} = 4 mA. Calculate : [10]

(1) I_{DSQ}

(2) V_{GSQ}

(3) V_{DSQ}.

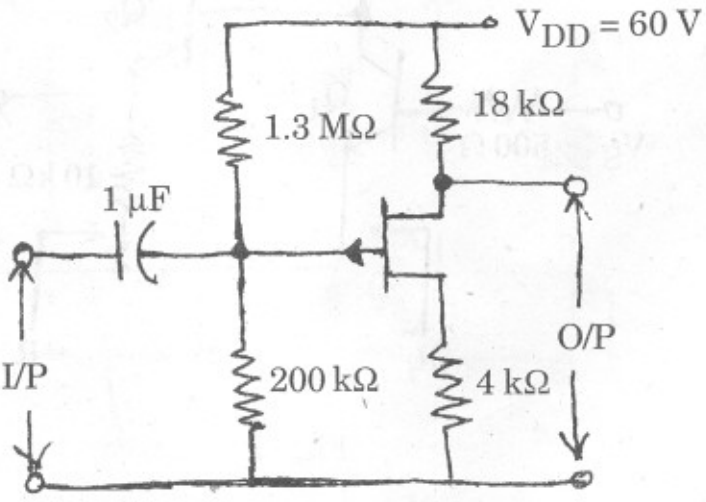

Fig. 3

9. (*a*) Draw block schematic of an Op-Amp and briefly explain function of each block. [8]

(*b*) What is Schmitt trigger ? What are threshold levels and hysteresis ? Explain with neat circuit diagram. [8]

Or

10. (*a*) How can Op-Amp be used as an inverting amplifier ? Derive an expression for its output and gain. [8]

(*b*) Draw and explain triangular waveform generator using Op-Amp 741. [8]

11. (*a*) Draw and explain *two* transistor model of SCR. Also explain regenerative action in SCR operation. [8]

(*b*) Draw and explain stepdown (Buck) switching regulator with regulating action. [8]

Or

12. (*a*) Draw and explain online and line interactive UPS. [8]

(*b*) Explain the construction and working of TRIAC. Sketch its V-I characteristic. [8]