T.E. (Computer) (2003 Course) (Semester – I) Examination, 2009
MICROPROCESSORS AND MICROCONTROLLERS

Time : 3 Hours Max. Marks : 100

Instructions : *1) In Section **I**, attempt Q. No. **1** or Q. No. **2**, Q. No. **3** or Q. No. **4**, Q. No. **5** or Q. No. **6**.*

*2) In Section **II**, attempt Q. No. **7** or Q. No. **8**, Q. No. **9** or Q. No. **10**, Q. No. **11** or Q. No. **12**.*

*3) Answers to the **two** Sections should be written in **separate books**.*

*4) Neat diagrams must be drawn **wherever** necessary.*

*5) **Black** figures to the **right** indicate **full** marks.*

*6) Assume suitable data, **if necessary**.*

SECTION – I

1. a) Discuss whether Pentium is a RISC or CISC microprocessor. Justify your answer. **6**

   b) How real address mode of Pentium is different than 8086 microprocessor ? **5**

   c) Describe on chip cache organisation of Pentium. **5**

OR

2. a) What are instruction pairing rules in Pentium for integer and floating point instructions ? **8**

   b) Which different data types for real numbers are supported by floating point unit of Pentium ? **4**

   c) What is the function of following pins ?

   1) NA# 2) AP **4**

3. a) What are privileged instructions ? Give two examples. 6
   b) Draw programmer's model of Pentium. 4
   c) How pipelined bus cycles are different than non pipelined bus cycles ? Explain with timing diagram. 6

OR

4. a) Which pins of Pentium are checked to decide the mode it enters after RESET ? 6
   b) Describe following instructions :
      1) SGDT 2) ARPL. 4
   c) Draw and explain how 16 bit memory is interfaced with Pentium. 6

5. a) Which different system descriptors are placed in GDT ? 4
   b) Describe the linear to physical address translation for 4 MB pages in Pentium with the help of diagram. 8
   c) What is the significance of CPL, RPL and DPL while accessing other code and data segments ? 6

OR

6. a) Describe the call gate mechanism in details. Draw the related descriptor formats. 8
   b) Describe logical to linear address translation in protected mode in Pentium using segmentation. 6
   c) Describe PDE and PTE formats. 4

SECTION – II

7. a) What are the contents of TSS ? Discuss the use of TSS in multitasking. 8
   b) What is I/O permission bit map ? Under which circumstances is it referred by Pentium ? 6
   c) What are error codes ? What is their use ? 4

OR

8. a) Describe IDT in Pentium in details. How interrupt handling in protected mode is dependent on contents of IDT ? 8
   b) How virtual 8086 mode is different than protected mode in Pentium ? 6
   c) Explain nested tasks in Pentium. 4

9. a) Describe various timer modes supported by 8051 microcontroller. **8**

   b) What is program status word (PSW) ? Describe its format. **4**

   c) What are the functions of $\overline{EA}$ and $\overline{PSEN}$ pins ? **4**

OR

10. a) Draw and explain architecture of 8051 microcontroller. **8**

    b) Discuss interrupt structure of 8051 in details. **8**

11. a) Describe the features of PIC 16C61 / 16C71. **6**

    b) Explain the working of watchdog timer in PIC 16C6X/7X in details. **6**

    c) Describe following SFRs :

    1) INDF 2) TRISA **4**

OR

12. a) Draw and explain memory banks supported by PIC 16C6X/7X. **6**

    b) Describe the significance of different bits that control the timer operation in PIC. **6**

    c) Explain the following instructions :

    1) bsf STATUS, 05 2) retfie. **4**
