Total No. of Questions—**12**] [Total No. of Printed Pages—**7**

[3562]-202

S.E. (Computer Engg.) EXAMINATION, 2009

ELECTRONIC DEVICES AND CIRCUITS

(2003 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer Questions **1** *or* **2**, **3** *or* **4** and **5** *or* **6** from Section I and Questions **7** *or* **8**, **9** *or* **10** and **11** *or* **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Compare fixed bias, collector to base bias and self bias circuits with respect to : [8]

(*i*) Circuit diagram

(*ii*) Biasing resistance/s and its location

(*iii*) Pretence of negative feedback

(*iv*) Equation for stability factors.

P.T.O.

(*b*) An *npn* silicon transistor operates in a self bias circuit with R_E = 1 kΩ, R_1 = 65 kΩ, R_2 = 15 kΩ and I_C = 1 mA at 10°C. Calculate variation in I_C over the temperature range of 10°C to 100°C.

The transistor parameters at 10°C and 100°C are as shown in the table below : [10]

Parameter	10°C	100°C
I_{CO} (μA)	0.01	1.2
V_{BE} (V)	0.74	0.54
β	30	70

Or

2. (*a*) Explain diode bias compensation and thermistor bias compensation. [8]

(*b*) For the collector to base bias with emitter bias, V_{CC} = 24 volts, R_C = 10 kΩ, R_E = 270 Ω. The transistor used has β = 45. If under quiescent conditions, V_{CE} = 5 V and V_{BE} = 0.6 V, calculate the value of R_B and stability factors. [10]

3. (*a*) Explain with neat diagram Miller theorem. Derive equation for effective input and output impedances. [2+4]

(*b*) The transistor used in Fig. 1, has h_{ie} = 500 Ω, h_{re} =

2.4×10^{-4}, $h_{fe} = 60$, $h_{oe} = \frac{1}{40 \times 10^3}$ ʊ (25 μA/V). Calculate R_i, R_i', A_i, A_V, A_{VS} and A_{is}. Assume all capacitors to be very large. [10]

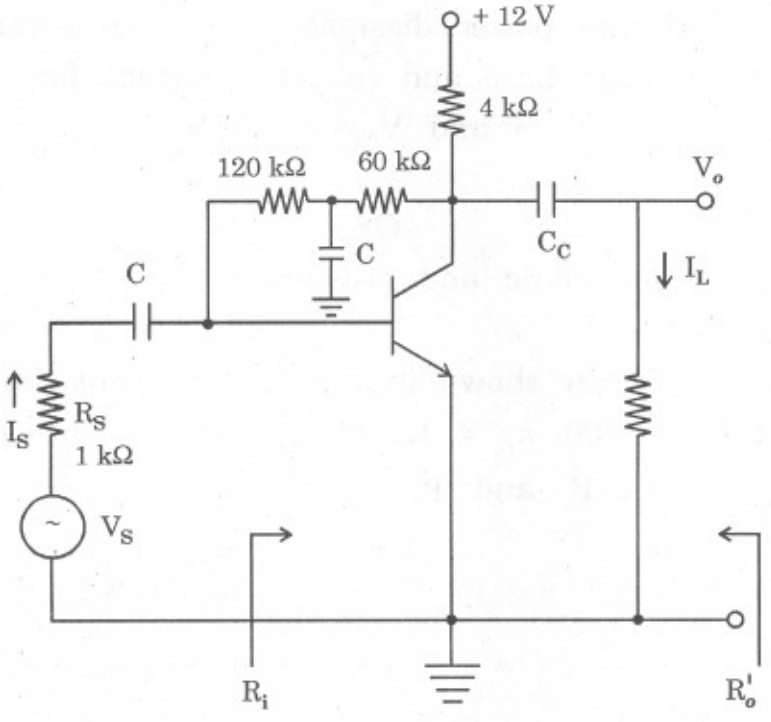

Fig. 1

Or

4. (*a*) Write a short note on high input impedance circuit. [6]

(*b*) For a transistor operating in common collector configuration with resistances R_1, R_2 and R_E, input source V_S and output voltage V_o, derive the expression for : [10]

(*i*) R_i and R_i'

(*ii*) R_o and R_o'

(*iii*) A_I and A_V

Use small signal analysis approach with necessary hybrid model.

5. (*a*) Explain various types of coupling in multistage amplifiers. [6]

(*b*) A class B push-pull amplifier supplies power to a resistive load of 12 Ω. The output transformer has a turns ratio of 3 : 1 and efficiency of 78.5%. Obtain :

(*i*) Maximum power output

(*ii*) Maximum power dissipation in each transistor

(*iii*) Maximum base and collector current for each transistor.

Assume h_{fe} = 25 and V_{CC} = 20 V. [10]

Or

6. (*a*) Explain harmonic and cross-over distortion in large signal amplifiers. [6]

(*b*) For the circuit shown in Fig. 2, the transistors are identical with h_{fe} = 100, h_{ie} = 1.1 kΩ, h_{oe} and h_{ve} are negligible. Find out A_i, A_v, R_i and R_o'. [10]

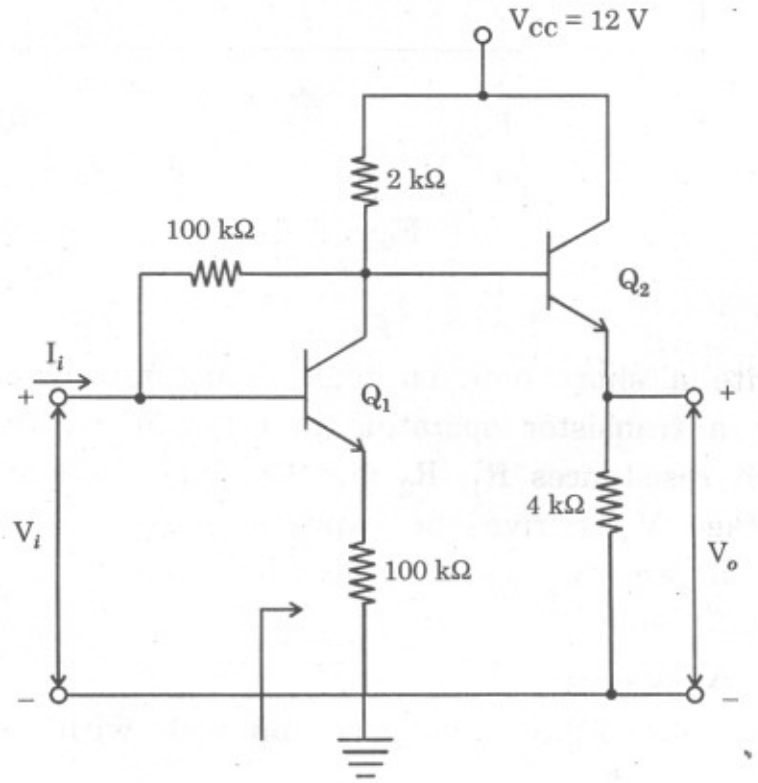

Fig. 2

SECTION II

7. (*a*) Explain the working of n-channel JFET and define the following : [8]

(*i*) gm—forward transconductance

(*ii*) rd—Drain resistance

(*iii*) ru—Amplification factor.

(*b*) Define pinch-off voltage. Determine the drain current and transconductance of n-channel MOSFET having

Pinch-off voltage = 4 volts, I_{dss} = 12 mA and gate to source voltage Vols = – 2 volts. [8]

Or

8. (*a*) Compare JFET and BJT. Explain the physical construction of depletion MOSFET and its working. [8]

(*b*) Explain the different regions of operation in the output characteristics of JFET and explain in which region JFET can work as amplifier and why ? And also draw the static and transfer characteristics of a JFET. [8]

9. (*a*) (*i*) Draw the circuit diagram of instrumentation amplifier using three operational amplifier (Op-Amp). [2]

(*ii*) State the characteristics/salient points of an Instrumentation amplifier and derive the expression for output voltage. [6]

(*b*) Give definition and typical values of operational amplifier parameters : [8]

(*i*) Input bias current

(*ii*) Input offset voltage

(*iii*) CMRR

(*iv*) Slew rate.

Or

10. (*a*) Explain necessity of precision rectifier ? Draw the circuit diagram of half wave rectifier ? And sketch its input output waveforms ? [8]

(*b*) The specification of dual input unbalanced output differential amplifier are : [8]

$R_C = 2.7\ k\Omega$, $R_{S1} = R_{S2} = 50\ \Omega$, $V_{CC} = 10$ V, $-V_{EE} = -10$ V, $\beta_{DC} = 100$ and $V_{BE} = 0.7$ volts.

Determine :

(*i*) I_{CQ} and V_{CEQ}

(*ii*) Voltage gain

(*iii*) Input and output resistance.

Assume both the transistors are identical.

11. (*a*) Explain the reasons for which the device is given name SCR. State its features. Draw the schematic diagram and a symbol of SCR. [6]

(*b*) Explain the schematic diagram, the working of DIAC and also sketch its V-I characteristics. [6]

(*c*) Explain what you mean by latchup in IGBT and how it can be avoided. [6]

Or

12. (*a*) Explain with neat circuit diagram, the operation of Boost converter. Derive equation for output voltage V_o. [6]

(*b*) Explain with neat circuit diagram, the operation of ONLINE UPS. State its specifications. [6]

(*c*) Explain in detail V-I characteristics and an applications of TRIAC. [6]