P1070

[3864]-244

B.E. (Electronics)
VLSI DESIGN
(2003 Course)

Time : 3 Hours]

[Max. Marks : 100

Instructions to the candidates:

    1)   Answer any three questions from each section.

    2)   Answers to the two sections should be written in separate books.

    3)   Neat diagrams must be drawn wherever necessary.

    4)   Figures to the right indicate full marks.

    5)   Use of logarithmic tables, slide rule, Mollier Charts, electronic pocket calculator and steam tables is allowed.

    6)   Assume suitable data, if necessary.

SECTION - I

Q1) What is function and procedures? Explain both these terms with suitable VHDL examples. [16]

OR

Q2) List synthesizable and Non synthesizable VHDL statements. Write HDL code for Mux 8:1 in two modelings. [16]

Q3) Draw state diagram and write HDL code for Traffic Light control. [16]

OR

Q4) What is metastability? Explain different methods of state minimization.

[16]

Q5) With block diagram explain detail architecture of CPLD [18]

OR

Q6) With block diagram explain detail architecture of FPGA. [18]

SECTION - II

Q7) Explain with schematic different types of memory. [16]

OR

Q8) Explain in short clock distribution, power distribution and global, switch box routing. [16]

Q9) a) What is technology scaling explain different scaling techniques? [9]

b) Explain different power dissipation in CMOS inverter. [9]

OR

Q10) Draw and explain voltage transfer characteristics of CMOS inverter and also derive (W/L) ratio between PMOS and NMOS transistor. [18]

Q11) What is the need of design for testability explain fault coverage, controllability and observability? [16]

OR

Q12) a) Explain with block diagram BIST. [6]

b) Draw state diagram and explain the functioning of TAP controller. [10]

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