Total No. of Questions—**12**] [Total No. of Printed Pages—4

[3862]-219

S.E (Computer Engineering) (Second Sem.) EXAMINATION, 2010

COMPUTER ORGANIZATION

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. **:—** Answer any *three* questions from Section-I and *three* questions from Section-II.

SECTION I

1. (*a*) With neat diagram explain in detail functional units of computer system. [8]

(*b*) Perform division of the following number using restoring and non-restoring algorithm : [10]

dividend = 1011

divisor = 0011.

Or

2. (*a*) Multiply the following pair of signed two's complement numbers using Booth's Algorithm : [8]

Multiplicand = 110011

Multiplier = 101100.

(*b*) Represent the following numbers into single precision and double precision format : [10]

(*i*) 309.1875

(*ii*) 178.1875.

P.T.O.

3. (a) Explain with suitable example how the size of the control words can be reduced to obtain small store. [8]

(b) Write control sequence for the execution of the following instruction : [8]

CALL SUB1

Or

4. (a) Give the comparison between : [8]

(i) Hardwired and Micro-programmed control.

(ii) Horizontal and Vertical Microinstructions.

(b) Explain briefly :

(i) Delay-element method [4]

(ii) Explain applications of Micro-Programming. [4]

5. (a) Explain register organization of 8086. [8]

(b) List and explain various ways in which an instruction pipeline can deal with conditional branch instructions. [8]

Or

6. (a) Discuss in detail instruction formats of INTEL/MOTOROLA processor. [8]

(b) Explain instruction cycle. How will you represent instruction cycle with interrupts ? Explain. [8]

SECTION II

7. (*a*) What is virtual memory concept ? Explain the role of TLB in virtual memory organization. [8]

(*b*) Explain in brief the following secondary storages : [10]

(*i*) DAT

(*ii*) RAID

(*iii*) CDROM

(*iv*) DVD.

Or

8. (*a*) Explain chache coherence strategies. [8]

(*b*) Explain how a memory address is mapped into a cache memory address using set associative mapped cache. The main memory is 64 K words, the cache memory has 2048 words with block size of 128 words. (use 2-way set associative memory technique). [10]

9. (*a*) Explain synchronous and asynchronous bus in an input operation with timing diagram. [8]

(*b*) Explain programmed I/O and interrupt driven I/O. [8]

Or

10. (*a*) Explain in detail DMA data transfer modes. [4]

(*b*) Explain in detail how scheduling and memory management is done by operating system with its types. [8]

(*c*) Explain : SCSI. [4]

11. (*a*) Explain in detail superscalar architecture. [8]

(*b*) Explain in detail bus arbitration techniques. [8]

Or

12. (*a*) Draw and explain architecture of a typical RISC processor. [8]

(*b*) With respect to SPARC processor, explain : [8]

(*i*) SPARC register set

(*ii*) instruction set

(*iii*) instruction format.