[3862] – 403

S.E. (Computer Engineering) (Semester – I) Examination, 2010
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2003 Course)

Time : 3 Hours Max. Marks : 100

Instructions : *1) Answer **1** or **2**, **3** or **4**, **5** or **6** questions from Section **I** and **7** or **8**, **9** or **10**, **11** or **12** questions from Section – **II**.*
*2) Answers to the **two** Sections should be written in **separate** books.*
*3) Neat diagrams must be drawn **wherever** necessary*
*4) Black figures to the **right** indicate **full** marks.*

SECTION – I

1. a) Perform the following Hexadecimal substraction and show your answer in hexadecimal only. **8**
   i) $(245)_{Hex} - (199)_{Hex}$
   ii) $(A27)_{Hex} - (72\ A)_{Hex}$
   b) Explain in detail 4-bit Binary code to Grey code conversion using k-map and MSI circuit. **10**

OR

2. a) For a maximum 4-bit decimal number, obtain max. equivalent octal and hex number. **6**
   b) Explain the error correcting and detecting codes with suitable examples. **6**
   c) Explain various Boolean algebra rules with suitable example. **6**

3. a) Draw and explain 3-input TTL NAND gate circuit, also write various i/p, o/p state table. **10**
   b) Explain various characteristics of TTL logic families. **6**

OR

4. a) Give the classification of logic families and also explain characteristics of digital IC's. **8**
   b) Explain NOR Gate using CMOS logic. **8**

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5. a) Draw and explain Binary to 7-segment driver IC 7447. Differentiate with IC 7448. **8**

   b) What is priority encoder ? Design a priority encoder using NAND gate. **8**

OR

6. a) Explain the working of BCD adder using IC 7483. **8**

   b) Design and explain 16:1 mux using 4:1 mux IC. **8**

SECTION – II

7. a) Explain the Design of 4-bit synchronous counter using J-K flip flop. Also draw timing diagram. **12**

   b) Explain lock-out condition. Briefly explain its avoidance method. **6**

OR

8. a) Explain types of shift registers. Draw and explain working of any two. **8**

   b) Explain Ring Counter (4-bit) in detail. Differentiate with JOHNSON ring counter. **10**

9. a) Explain execution in VHDL. **4**

   b) Explain design steps of RTL. **4**

   c) What is ASM chart ? Explain the MUX controller method with suitable example. **8**

OR

10. a) Write entity-architecture declaration for 2-i/p x-NOR and NAND gate. Assume A and B as inputs and C as output of logic gates. **8**

    b) Draw ASM chart for 4-bit grey code sequence. **8**

11. a) What is PLD ? Explain in brief GAL, PAL and PLA. **8**

    b) Explain in detail PLA design. **8**

OR

12. Explain in detail CPLD architecture. Describe how to program CPLD. List available tools to design CPLD, and various design steps involved in it. **16**
