S.E. (Comp.) (Semester – I) Examination, 2010
ELECTRONIC DEVICES & CIRCUITS
(2003 Course)

Time : 3 Hours Max. Marks : 100

Instructions: *1) Answer **any three** questions from **each** Section.*
*2) Answers to the **two** Sections should be written in **separate** books.*
*3) **Neat** diagrams must be drawn **wherever** necessary.*
*4) Black figures to the **right** indicate **full** marks.*
*5) Use of electronic pocket calculator is **allowed**.*
*6) Assume suitable data, if **necessary**.*

SECTION – I

1. A) The circuit in fig. 1 uses a silicon transistor with current gain (β) 200 & V_{CEQ} = 3V. For the output voltage (V_o) to be zero
   i) Determine the value of collector resistance and emitter resistance. **8**
   ii) With reference to the values in part (1) above, find the new value of V_o if β is 100. **4**

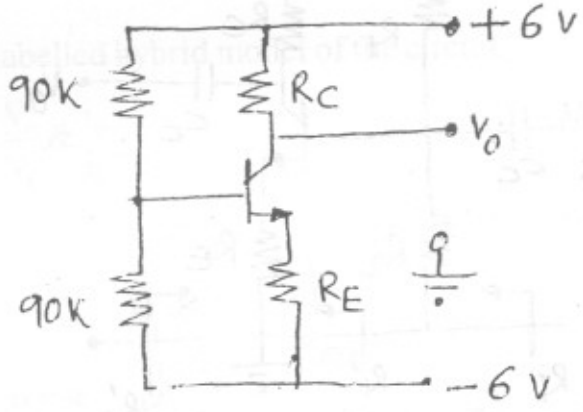

Fig. 1

B) Explain Thermal Runaway. **4**

OR

2. A) Calculate stability factor for a transistor circuit to be thermally stable if the specifications are as under
   - Transistor used is NPN and is operated in self bias arrangement
   - The component values are R_C = 1k and R_E = 0.1 K
   - The parameter values are I_{CO} = 1.2 nA, $\theta = 10 \times 10^8$ °C/W, V_{CEQ} = 5.5V
   - The power supply used is +10 volts. **8**

   B) Explain with necessary illustrations, what happens when
   i) Operating point is located closer to saturation region **4**
   ii) Operating point is located closer to cutoff region. **4**

3. A) For the circuit in fig. 2
   i) Draw the small signal hybrid model. **2**
   ii) Derive in terms of h parameter and circuit component the equations for a) current gain A_I and A_{IS} b) Voltage gain A_v and A_{VS} c) Input impedance R_i' and R_i d) output impedance R_O and R_o'. **10**

   B) Justify "CE is the only transistor configuration to produce phase shift between input and output signal". **4**

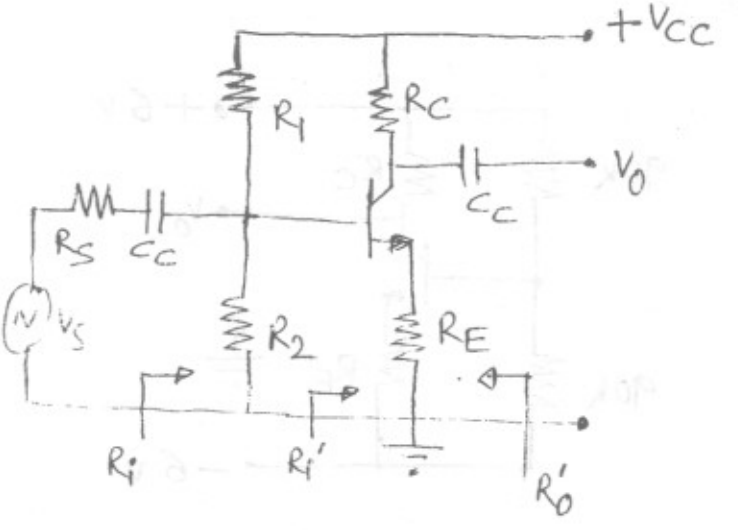

Fig. 2

OR

4. A) For the circuit in fig. (3), the transistor h parameters are hie = 1k, hfe = 50 and negligible hre and hoe, determine the following

i) $A_v = \frac{v_0}{v_s}$ ii) $A_i = \frac{i_o}{i_s}$ iii) R_i iv) R_0' **10**

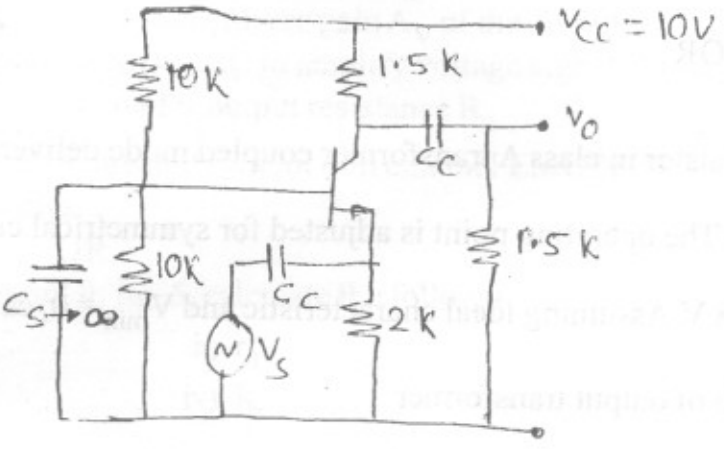

Fig. 3

B) Draw the circuit diagram and explain importance of **6**
   i) Bootstrap emitter follower circuit
   ii) Bootstrap darlington pair

5. A) For the circuit in fig. 4, transistors used are identical with hie = 2k, hfe = 100, hre = hoe = 0,
   i) Draw neat labelled hybrid model of the circuit. **2**
   ii) Determine $\frac{V_o}{V_s}$ & $\frac{i_o}{i_s}$. **8**

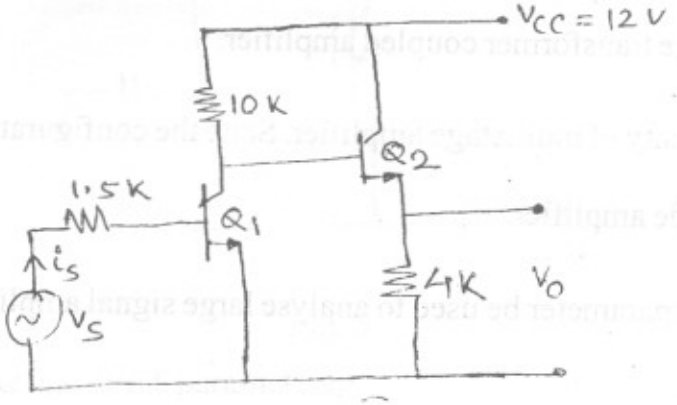

Fig. 4

B) Explain harmonic and cross over distortion of a power amplifier with necessary illustrations. 6

C) Explain what you mean by large signal and small signal. 2

OR

6. A) A power transistor in class A transformer coupled mode delivers 5W Power to $5\,\Omega$ load. The operating point is adjusted for symmetrical current swing with $V_{cc} = 18$ V. Assuming ideal characteristic and $V_{min} = 0$, calculate

i) turns ratio of output transformer

ii) peak collector current

iii) Q point coordinates

iv) collector circuit efficiency 8

B) Draw the circuit diagram of two stage

i) Direct coupled amplifier

ii) R-C coupled amplifier

iii) Single stage transformer coupled amplifier. 6

C) Explain necessity of multistage amplifier. State the configuration of stages used in cascade amplifier. 2

D) Explain can h parameter be used to analyse large signal amplifier. 2

SECTION – II

7. A) i) Draw the circuit diagram of a source follower n channel JFET, consisting of R_D, R_S, R_G, input source V_i and coupling capacitors C_C. **2**
   ii) Draw the small signal model of the circuit in part (1) above. **2**
   iii) Derive equation for drain current i_d **2**
   iv) Obtain equation for voltage gain A_V of the circuit. **2**
   v) Can this circuit be used to amplify voltage signal. Justify your answer. **2**
   vi) Derive equation for output resistance R_o **2**

   B) Draw the structure and symbol of n channel EMOSFET. Sketch its transfer characteristics. **4**

OR

8. A) For the circuit in fig. 5, calculate the following

   i) g_m ii) r_d
   iii) A_v iv) R_i v) R_o **10**

   Assume $I_{D(ON)}$ = 5.5 mA, $V_{GS}(ON)$ = 7.5V, V_T = 3V, Y_{OS} = 50 μs, k = 0.25 mA/v^2, V_{GS}= 6.5 V & I_D = 3 mA. Use Miller theorem. Calculate values of R_{eff}(i/p) and R_{eff}(o/p). **2**

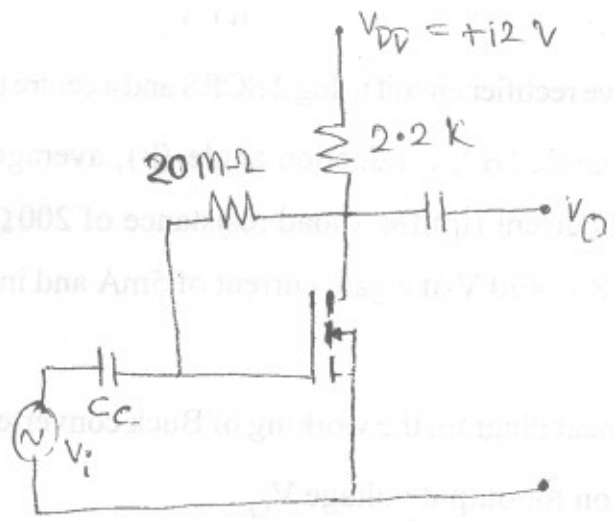

Fig. 5

B) State and define JFET parameters. **4**

9. A) i) Draw block diagram of OPAMP. 2

ii) Sketch the circuit of level shifter an derive equation for output voltage V_o. 4

iii) State disadvantage of level shifter and explain how it can be overcome with the help of necessary circuit. 4

B) Draw and explain operation of I to V converter circuit using OPAMP. Derive equation for output voltage V_o. State its application. 6

OR

10. A) i) Draw using OPAMP a circuit to generate a square wave without any input signal applied to it. 2

ii) Explain its operation with the help of waveforms V_C & V_O. 4

iii) Derive equation for time period T of the square wave. 4

B) Explain OPAMP parameters

i) CMRR ii) PSRR

iii) Slew rate iv) V_{io}. 6

11. A) i) Draw a full wave rectifier circuit using 2 SCRS and a centre tap transformer. 2

ii) Obtain firing angle (α), conduction angle (β), average output voltage (V_o) and load current (i_L) for a load resistance of 200 Ω if the forward voltage of SCR is 400 V at a gate current of 5mA and input applied is 600 sin wt. 6

B) i) Explain with neat diagram the working of Buck converter. 3

ii) Obtain equation for output voltage V_O 3

iii) Sketch the nature of output voltage waveform 2

C) Sketch V-I characteristic of diac 2

OR

12. A) i) State difference between on line and off line UPS. **2**

ii) Explain operation of on line UPS with neat diagram. **4**

B) i) Explain operation of SCR using two transistor analogy. **3**

ii) Derive equation for anode current I_A. **3**

C) Define i) Latching current ii) Holding current iii) V_{BO} iv) V_{BR}. **6**
