P1378   **[3764]-420**

B.E. (Computer)

ADVANCED COMPUTER ARCHITECTURE AND COMPUTING

(2003 Course) (410249)

Time : 3 Hours]   *[Max. Marks : 100*

Instructions to candidates :

  1) *Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6 from Section I and Q.7 or Q.8, Q.9 or Q.10, Q.11 or Q.12 from Section II.*
  2) *Answers to the two sections should be written in separate books.*
  3) *Neat diagrams must be drawn wherever necessary.*
  4) *Assume suitable data, if necessary.*

SECTION - I

Q1) a) How Feng has classified parallel computers? What is maximum Parallelism degree and how it is obtained? Why MISD Architecture suggested by Flynn does not popular? What is MISD? **[8]**

   b) State the EPIC features of Itanium Architecture. Why it is called as VLIW Architecture? **[8]**

OR

Q2) a) Define parallel processing. How parallel Computer Architectures are classified? Discuss the levels of parallel processing. **[8]**

   b) How the performance of parallel computer systems is measured in general? State and explain such parameters giving it's significance. **[8]**

Q3) a) For a unifunction pipeline, the forbidden set of latencies is given as follows: **[10]**

   F = {1, 3, 6} with largest forbidden latency = 6.

   i) Define and obtain Collision vector.

   ii) State the problem of Job sequencing / scheduling.

   iii) Draw the state diagram.

   iv) Define latency & MAL.

   v) Obtain MAL.

   vi) State all simple and greedy cycles.

   vii) Define Greedy cycle.

P.T.O.

b) What is Hazard? State and explain different types of data hazards. State how such hazards can be detected and resolved? [8]

OR

Q4) a) Consider a 4 stage pipeline processor. The number of clock cycles needed for the execution of four instructions I_1, I_2, I_3, I_4 in stages S_1, S_2, S_3, and S_4 is shown below– [8]

	S_1	S_2	S_3	S_4
I_1	2	1	1	1
I_2	1	3	2	2
I_3	2	1	1	3
I_4	1	2	2	2

Obtain the total number of clock cycles needed to execute the following loop–

    for   (i = 1 to 2)

        {

            I_1;

            I_2;

            I_3;

            I_4;

        }

Draw the space time diagram showing execution of all instructions through successive pipeline stages.

b) Explain loop unrolling technique with suitable example state it's advantages and disadvantages. Compare it with software pipelining. What is trace scheduling? [10]

Q5) a) State advantages of vector processing over scalar processing. What is vectorizing compiler? Explain any 2 vector optimizing functions. [8]

b) Discuss with algorithm the problem of n × n matrix multiplication on cube interconnection Network. Specify the complexity. [8]

OR

Q6) a) How 3-cube Network can be viewed as single stage recirculating Network? State the routing functions and permutation cycles for 3-cube Network. [8]

b) With the algorithm discuss the problem of parallel sorting of N elements on n × n mesh Interconnection Network. Obtain it's time complexity. **[8]**

SECTION - II

Q7) a) State the Cache write policies used in Cache coherency protocol. Discuss pentium MESI protocol with it's state diagram. **[8]**

b) With Neat diagram, compare and explain following bus Arbitration algorithms. **[10]**

    i) Daisy chaining.

    ii) Polling.

OR

Q8) a) What is chip-multiprocessing? With functional Block diagram, explain the architecture of IBM power 4 / power 5 processor. **[10]**

b) What is interprocess communication and synchronization? Discuss any two machine instructions which provides Hardware support for interprocess communication and synchronization. **[8]**

Q9) a) What is the necessity of memory consistency models? Explain in brief processor consistency models. **[8]**

b) State the following terms w.r.t. multithreading. **[8]**

    i) Latency.

    ii) Context switching overhead.

    iii) Interleaved Multithreading.

    iv) Number of active threads.

    v) Latency Hiding.

OR

Q10)a) Explain use of following primitives w.r.t. parallel programming. **[8]**

    i) Send ( ) ;

    ii) Receive ( ) ;

    iii) Fork ( ) ;

    iv) Join ( ) ;

    v) Lock ( ) ;

b) What are features of Data Parallel programming. Explain the standard constructs available in data parallel programming. [8]

*Q11)*a) What are features of PVM? How processes are created in PVM? Explain the communication functions defined under PVM. [8]

b) With example, explain how parallel algorithms are written for Multiprocessor systems. [8]

OR

*Q12)*a) State and explain control and data Parallelism used in CCC by means of standard constructs. [8]

b) Discuss and compare the architecture of Cluster and Grid computing.[8]