Total No. of Questions : 12] [Total No. of Pages : 02

P1480

[3764] - 244

B.E. (Electronics)

VLSI DESIGN

(2003 Course)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) *Answer any 3 questions from each section.*
2) *Answers to the two sections should be written in separate books.*
3) *Neat diagrams must be drawn wherever necessary.*
4) *Figures to the right indicate full marks.*
5) *Use of logarithmic tables, slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.*
6) *Assume suitable data, if necessary.*

SECTION - I

Q1) Using structural modeling draw schematic and write VHDL code of 16:1 Mux by 4:1 Mux (as a component). **[16]**

OR

Q2) a) List different synthesizable VHDL statements. **[4]**

b) Explain function and procedure with VHDL examples. **[12]**

Q3) Draw state diagram and write VHDL code for Traffic light control. **[16]**

OR

Q4) a) What is metastability and synchronization. **[6]**

b) Write VHDL code for Lift control. **[10]**

Q5) Draw detail block diagram and explain different sub-blocks of CPLD. **[18]**

OR

Q6) a) Draw only the block diagram FPGA and explain difference between CPLD and FPGA. **[12]**

b) Write specification of CPLD and FPGA. **[6]**

P.T.O.

SECTION - II

Q7) a) What is clock skew and Jitter? Explain different techniques of clock distribution. [12]

b) Define Global and switch Box routing. [4]

OR

Q8) a) Explain the classification of memory. [12]

b) Define off chip connection. [4]

Q9) a) What is technology scaling? Explain different scaling techniques. [12]

b) Explain what is body effect in MOSFET. [4]

OR

*Q10)*a) Explain different power dissipation in CMOS Inverter, also define power delay product. [12]

b) Draw schematic and explain Transmission Gate. [4]

*Q11)*a) What is the need of DFT? With schematic explain different faults. [12]

b) Define controllability and observability. [6]

OR

*Q12)*Write short notes on: [18]

a) TAP Controller.

b) BIST.

c) JTAG.