Total No. of Questions—**12**] [Total No. of Printed Pages—**4+2**

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S.E. (Computer Engineering) (First Sem.) EXAMINATION, 2010

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2003 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answers to the two Sections should be written in separate answer-books.

(*ii*) In Section I attempt Question Nos. **1** *or* **2**, **3** *or* **4**, **5** *or* **6** and in Section II attempt Question Nos. **7** *or* **8**, **9** *or* **10**, **11** *or* **12**.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Explain error detection and error correction. [6]

(*b*) Express the –45 and –116 decimal numbers in :

(*i*) Sign Magnitude form

(*ii*) One's Complement and

(*iii*) Two's Complement form.

Assume 8 bit word length. [6]

(*c*) Perform $(-17)_{10} - (+27)_{10}$ using the 2's complement method. [2]

(*d*) Differentiate between Binary Code and Gray Code. [4]

P.T.O.

Or

2. (*a*) List the procedure to detect and correct error in the received Hamming Code. If A seven bit even parity Hamming Code is Received as 1100110, what is the correct code ? [6]

(*b*) List the following Boolean Laws :

(*i*) Commutative Laws

(*ii*) Distributive Laws

(*iii*) Associative Laws

(*iv*) Inverse Law. [6]

(*c*) Perform the following using binary arithmetic :

(*i*) Multiply $(16)_{10}$ by $(9)_{10}$

(*ii*) Divide $(45)_{10}$ by $(7)_{10}$. [2]

(*d*) Explain De Morgan's Theorem using truth table and example. [4]

3. (*a*) Differentiate between TTL and CMOS w.r.t. :

(*i*) Fan in

(*ii*) Fan out

(*iii*) Power dissipation per gate

(*iv*) Propagation delay

(*v*) Figure of merit

(*vi*) Power supply voltage. [6]

(*b*) Explain TTL NAND gate with totem pole output. Explain multi-emitter transistor in it. [6]

(*c*) Define the following parameters and give the typical values of these parameters w.r.t. CMOS logic family :

(*i*) Sourcing Current

(*ii*) Sinking Current. [4]

Or

4. (*a*) What is the drawback of WIRED_OR TTL Gate ? Exlain, how it can be removed usnig TRI_STATE Gate. [6]

(*b*) Define noise margin and figure of merit w.r.t. TTL. Give their significance. [6]

(*c*) Comment on Power dissipation and propagation delay of H, L, S and LS 7400 series. [4]

5. (*a*) Write short notes on :

(*i*) IC 74138

(*ii*) IC 74151. [8]

(*b*) Explain BCD adder using IC 7483. [8]

Or

6. (*a*) Design 16 : 1 MUX using 2 : 1 MUX only. Draw truth table and explain design procedure. [6]

(*b*) Realize the following logic function in SOP form using Quine-Mc Cluskey method and find all prime implicants :

$F(P, Q, R, S) = \Pi . M(0, 2, 3, 7, 5, 9, 10, 14, 13) . d(1, 4, 8)$. [10]

SECTION II

7. (*a*) Design MOD-11 asynchronous counter. Draw timing diagram. [8]

(*b*) Design a Sequence Detector 101 using Moore state m/c. Use D flip-flops.

(*i*) Draw the state diagram.

(*ii*) Write the state table.

(*iii*) Write Excitation Table for DFF.

(*iv*) Write circuit Excitation Table.

(*v*) K-maps and simplifications.

(*vi*) Draw Logic Circuit diagram. [10]

Or

8. (*a*) Explain race around condition. How can it be avoided ? [4]

(*b*) Give the names of the following IC's :

(*i*) IC 7473

(*ii*) IC 7476

(*iii*) IC 7490

(*iv*) IC 74373. [4]

(c) Design a Sequence Generator 1100010 using JKFFs.

(i) Draw the state diagram.

(ii) Write the state table.

(iii) Write Excitation Table for JKFF.

(iv) Write circuit Excitation Table.

(v) K-maps and simplifications.

(vi) Draw Logic Circuit diagram. [10]

9. (a) What is RTL ? Explain the following RTL Notations and Implementation :

(i) Transfer of contents of one Register to the other.

(ii) A conditional transfer.

(iii) Two or more operations at the same time. [8]

(b) Draw the ASM chart for a 3 binary DOWN COUNTER having one enable line E such that :

E = 1 (counting enabled), E = 0 (counting disabled).

Also draw state diagram. [4]

(c) Differentiate between concurrent and sequential statement w.r.t. VHDL. [4]

Or

10. (a) Explain Structural and Behavioural modeling of VHDL. [4]

(*b*) Explain, in detail, ASM technique of designing the sequential circuit using MUX controlled method. How does it differ from conventional flow chart ? [8]

(*c*) Explain process statement using syntax and *one* example. [4]

11. (*a*) Implement the following functions using PLA :

$$A(P, Q, R) = \Sigma m(0, 1, 6, 7)$$

$$B(P, Q, R) = \Sigma m(1, 2, 4, 6)$$

$$C(P, Q, R) = \Sigma m(2, 6).$$ [8]

(*b*) Write a short note on Xilinx XC 4000 FPGA family. [4]

(*c*) Explain difference between PLA and PAL. [4]

Or

12. (*a*) Draw and explain block diagram of CPLD. [6]

(*b*) How can we expand the PLA capacity for :

(*i*) Number of outputs

(*ii*) Number of product terms. [6]

(*c*) Draw and explain Configurable PAL. [4]