Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

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S.E. (Information Technology) (II Sem.) EXAMINATION, 2010

PROCESSOR ARCHITECTURE AND INTERFACING

(2008 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer Question Nos. **1** *or* **2, 3** *or* **4** and **5** *or* **6** from Section I and Question Nos. **7** *or* **8, 9** *or* **10** and **11** *or* **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Write features of 80386. Draw real mode register set of 80386 and explain their function. [10]

(*b*) Explain significance of the following signals of 80386 : [8]

(*i*) $D/\overline{C}$

(*ii*) $\overline{ERROR}$

(*iii*) NMI

(*iv*) $\overline{READY}$.

Or

2. (*a*) State and explain any *five* memory addressing modes of 80386 with example showing physical address generation. [10]

(*b*) Draw timing diagram of write machine cycle for 80386. Show status of important signals and list activities carried out in sequence. [8]

P.T.O.

3. (*a*) What are the components of MS-DOS ? What is the difference between DOS and BIOS interrupts or calls. [8]

(*b*) Compare and contrast : [8]

(*i*) Procedure and Macro

(*ii*) FAR & NEAR Call.

Or

4. (*a*) Draw Interfacing diagram to interface a 4 × 4 Hex keyboard to 8255. Find control word of 8255 for this interface. Write an algorithm to detect key press using keyboard scanning method. [8]

(*b*) State the syntax and mention operations carried out by 80386 microprocessor to execute the following instructions : [8]

(*i*) XLAT

(*ii*) CWD

(*iii*) LOOP

(*iv*) REP.

5. (*a*) With neat diagrams explain process of address translation in protected mode of 80386 when paging is enabled. [10]

(*b*) Write difference between real and protected mode of 80386 with respect to : [6]

(*i*) Memory segmentation

(*ii*) Physical address generation

(*iii*) Instruction set.

Or

6. (*a*) What is DPL, RPL and CPL ? Write privilege checks performed by 80386 while accessing code or data with protection mechanism. [10]

(*b*) What is descriptor cache ? When are they accessed by 80386 ? What is its use ? [6]

SECTION II

7. (*a*) CALL gate acts as an interface layer to a code with different privilege levels. Justify the statement with the help of CALL gate descriptor. [8]

(*b*) Specify size and function of LDTR, IDTR and TR. [6]

(*c*) Write stack related steps performed by 80386 processor in executing an inter-level CALL. [4]

Or

8. (*a*) What is TSS and TSS descriptor ? Explain the function and reaction of 80386 when the task switch occurs. [8]

(*b*) What is the different between the Trap gate descriptor and the interrupt gate descriptor ? [6]

(*c*) What is confirming code segment ? [4]

9. (*a*) Draw and explain functional block diagram of 8051. [8]

(*b*) Compare with respect to use and operations carried out by 8051 : [8]

(*i*) RET & RETI

(*ii*) SJMP & AJMP.

Or

10. (*a*) State and justify addressing mode of the following 8051 instructions : [8]

(*i*) MOVX A, @DPTR

(*ii*) MOVC A, @A + PC

(*iii*) ADD A, #10

(*iv*) MUL AB.

(*b*) List interrupts supported by 8051 with their vector addresses and default priorities. Explain interrupt programming with the help of IE and IP special function registers. [8]

11. (*a*) State timer modes of 8051 and explain timer programming of mode 1 for baud rate generation in serial communication with the help of TMOD & TCON SFRs. [8]

(*b*) List the features of PIC microcontroller and write a comment on Harward architecture of PIC microcontroller. [8]

Or

12. (*a*) Draw asynchronous serial communication format. Explain SCON, SBUF & PCON special function registers and their utility. [8]

(*b*) Write 8051 algorithm to generate square wave of 2 kHz frequency with ISR based timer programming in mode 2. Show calculations involved. Assume crystal frequency of 11.0592 MHz. [8]