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T.E. (Computer) (Semester – I) Examination, 2010
MICROPROCESSORS AND MICROCONTROLLERS
(2003 Course)

Time : 3 Hours Max. Marks : 100

Instructions : *1) In Section **I**, attempt Q. No. **1** or Q. No. **2**, Q. No. **3** or Q. No. **4**, Q. No. **5** or Q. No. **6**.*
*2) In Section **II**, attempt Q. No. **7** or Q. No. **8**, Q. No. **9** or Q. No. **10**, Q. No. **11** or Q. No. **12**.*
*3) Answers to the **two** Sections should be written in **two separate** books.*
*4) **Neat** diagrams must be drawn **wherever** necessary.*
*5) Figures to the **right** indicate **full** marks.*
*6) Assume suitable data **if necessary**.*

SECTION – I

1. a) Describe integer pipelining stages in Pentium microprocessor. **6**

   b) What is the role of prefetch buffers and Branch Target Buffer in Pentium Processor ? **6**

   c) List RISC features of Pentium. **4**

   OR

2. a) Which additional registers are available in real address mode of Pentium than true 8086 ? **4**

   b) Explain the following Pins **6**
      i) FLUSH#
      ii) $\overline{KEN}$
      iii) $\overline{FERR}$

   c) Describe Data Cache organization of Pentium in details. **6**

P.T.O.

3. a) Draw and explain memory interfacing and data transfer mechanism for 32 bit Memory with Pentium. 8

   b) Describe different addressing modes in Pentium along with suitable examples. 8

OR

4. a) What is BIST ? How does Pentium enter BIST ? 6

   b) Draw and explain Pipelined bus Cycle of Pentium. 6

   c) Describe following instructions : 4

      i) CMPXCHG8B

      ii) INS

5. a) Describe Logical to Linear address translation mechanism in Pentium. Draw the required data structures. 8

   b) Which bits of PDE and PTE provide Page Level Protection in Pentium ? 6

   c) How privileged instructions are different than protected mode instructions ? 4

OR

6. a) What is the use of control registers ? Explain significance of CR0 in working of Cache and Paging unit. 8

   b) What are privilege level protections rings in Pentium ? State the rules of accessing 1) Other data segment 2) Non Conforming Code Segment 6

   c) Explain significance of Granularity bit, limit field in Segment Descriptor. 4

SECTION – II

7. a) Explain the significance of IOPL field in Pentium ? When does Pentium refer I/O permission bit map ? 6

   b) What is Task ? Explain the steps performed by Pentium to switch to a new task. 8

   c) What are different classes of exception ? 4

OR

8. a) Describe different Descriptors found in IDT. How interrupts are handled by Pentium depending on those descriptors ? **8**

   b) Explain Virtual mode in Pentium. How does Pentium enter Virtual mode ? **6**

   c) Describe the following instructions : **4**
      i) SGDT
      ii) LTR

9. a) What are different addressing modes in 8051 ? Explain with suitable example. **8**

   b) What are different sources of interrupts in 8051 ? Explain interrupts handling mechanism. **8**

OR

10. a) Describe internal and external data memory organization of 8051 in details. **8**

    b) Describe the Serial port in 8051 with the help SCON register. **8**

11. a) Describe Power on Reset and Brown out Reset in PIC Microcontroller. **6**

    b) Draw and explain architecture of PIC 16C61/71. **8**

    c) Explain the CLRWDT instruction. **2**

OR

12. a) How many I/O ports are available in PIC 16C61/71 ? Which registers are used to configure them ? **6**

    b) Explain PWM mode of Timer in PIC 16C61/71. **6**

    c) Explain the following instructions : **4**
       i) BTFSC
       ii) MOVLW.
