Total No. of Questions : 12]

SEAT No. :

[Total No. of Pages : 3

P2100

B.E. (Semester - I)
VLSI DESIGN
Electronics Engineering
(2008 Pattern)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6 from Section - I & Q.7 or Q.8, Q.9 or Q.10, Q.11 or Q.12 from Section - II.***
3) ***Answer any three questions from each section.***
4) ***Neat diagrams must be drawn wherever necessary.***
5) ***Figures to the right side indicate full marks.***
6) ***Use of Calculator is allowed.***
7) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explain the transmission gate. Design Y = AC + AD + B using transmission gate. State the advantages of transmission gate over conventional gates. **[8]**

b) Explain technology scaling. Describe the various effect of scaling on the wires, memory, time, architecture. **[8]**

OR

Q2) a) Explain the static & dynamic power dissipation. Derive an expression for power delay product. **[8]**

b) Explain CMOS inverter and its transfer characteristics in detail. How to achieve symmetry in these characteristics. **[8]**

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Q3) a) Explain SRAM in detail with suitable diagram. **[8]**

b) Differentiate between SRAM & DRAM technologies. **[8]**

OR

Q4) a) Give the classification of memory with the application in each case. **[8]**

b) Explain DRAM in detail. **[8]**

Q5) a) Write a VHDL code for a 4 bit Up/Down counter. Also write a test bench for it. **[9]**

b) Compare synthesizable and non-synthesizable statements with examples. **[9]**

OR

Q6) a) Differentiate Moore and Mealy machine with suitable examples. **[9]**

b) Explain with example(s) data types and objects types in VHDL. **[9]**

SECTION - II

Q7) a) Differentiate the logic implementation between CPLD and FPGA. **[8]**

b) With neat schematic, explain the architectural building blocks of FPGA. Give limitations of FPGA over CPLD. **[8]**

OR

Q8) a) Draw & explain CMOS architecture of SRAM. **[8]**

b) Compare between PLDS, CPLDs, FPGAs and ASICS. **[8]**

Q9) a) What are the types of fault? Explain with schematic. **[8]**

b) Explain JTAG. What are the various pins involved? **[8]**

OR

Q10) a) What are objectives of boundary scan techniques? Explain boundary scan in detail. **[8]**

b) Explain TAP controller with state diagram. **[8]**

Q11) a) What it the need of check rule? Explain SRC and DRC with their limitations. **[9]**

b) What is power optimization? Explain the methods of optimization at various levels. **[9]**

OR

Q12) a) What are the problems in one phase clock? Explain the concept of two phase clock with example. **[9]**

b) Explain the following terms : **[9]**

Switch Box Routing.

Global Routing.

Power distribution.