Total No of Questions: [12] *SEAT NO. :* [ ]

[Total No. of Pages : 2]

S.E. (Computer) 2008 Course
Computer Organization
Semester II(May 2014) 2008 Course

Time: 3 Hours *Max. Marks : 100*

Instructions to the candidates:

1) *Answers to the two sections should be written in separate answer books.*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right side indicate full marks.*
4) *Assume Suitable data if necessary*

SECTION I

Q1) a) Explain the general architecture of IAS. [8]

b) Draw the flowchart for restoring unsigned division algorithm and divide the following numbers using the same algorithm and justify your answer [10]
Dividend= 22, Divisor = 6

OR

Q2) a) Represent the following numbers into single precision and double precision format. [10]
i. 208.1875
ii. 135.76

b) Multiply the following pair of numbers using Booth's algorithm method. [8]
Multiplicand= -12
Multiplier=6

Q3) a) What is addressing mode? Explain different addressing modes detail with suitable example [8]

b) What is the segmentation? Discuss the different segmentation schemes in 8086. [8]

OR

Q4) a) Explain instruction cycle with the help of state diagram. [8]

b) Write difference between data hazard and instruction hazard. [8]

Q5) a) Draw and explain the instruction format of 8086. [8]

b) Enlist different design methods of Hardwired Control unit. Explain any one. [8]

OR

Q6) a) Write control sequence for an unconditional branch instruction [4]

b) Give an example of Micro programmed control instructions [6]

SECTION –II

Q7) a) What is physical address? Explain the procedure of converting Virtual address to Physical address with suitable diagram. [10]

b) What is cache coherency? Discuss its advantages in Computer Science. [8]

OR

Q8) a) List and explain policies used with cache memory and state write policy for virtual memory with justification [10]

b) Explain the RAID2 scheme with suitable example. [8]

Q9) a) Explain the working principle of the following: [8]

1. Display Devices
2. Scanners

b) What is the use of DMA? What is the cycle stealing in DMA? [8]

OR

Q10) a) Explain the SIMD and MIMD architecture with suitable diagram. [8]

b) What is interrupt? Differentiate vectored and non vectored interrupts. [8]

Q11) a) Explain NUMA cache coherency method in detail. [8]

b) Differentiate RISC and CISC architectures. [8]

OR

Q12) a) What are the methods of bus arbitration? Explain polling method of bus arbitration with a diagram. [8]

b) Write short notes on followings [8]

i. Superscalar Architecture

ii. Array Vector Processor