Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

Seat No.	

S.E. (I Sem.) (Computer) EXAMINATION, 2014

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answers to the two Sections should be written in separate answer-books.

(*ii*) Answer any *three* questions from each Section.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Use of calculator is allowed.

(*vi*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Convert the following numbers into its equivalent decimal and hex : [6]

(*i*) $(122)_8$

(*ii*) $(176)_8$.

(*b*) Realize the following equations using K-Map minimization technique : [12]

(*i*) $Z = f(A, B, C, D) = \pi(0, 1, 2, 6, 8, 9, 10)$

(*ii*) $Z = f(A, B, C, D) = \Sigma(0, 1, 2, 3, 7, 8, 9, 10, 11, 15)$.

P.T.O.

Or

2. (*a*) What will be the Excess-3 code of any given 4-Bit BCD number ? Convert 4-Bit Excess-3 Code into corresponding BCD code. Show truth table and draw MSI circuit. [8]

(*b*) Convert a number $(F4A)_{16}$ to a number with base 2 and convert a number (111010011110) to a number with base 8. [6]

(*c*) With suitable example, explain the following in Boolean algebra : [4]

(*i*) Associative Law

(*ii*) Distributive Law.

3. (*a*) With the help of Quine-McClusky technique solve the following equation :

$Z = f(A, B, C, D) = \Sigma(0, 3, 4, 9, 10, 12, 14)$

Draw circuit diagram. [10]

(*b*) Explain standard CMOS characteristics in brief. [6]

Or

4. (*a*) Draw 2-i/p standard TTL, NAND gate with Totem Pole. Explain operation of transistor (ON/OFF) with suitable input conditions and truth table. [10]

(*b*) What is logic family ? Explain the types of logic families in detail. [6]

5. (*a*) Draw and explain 4-bit BCD subtractor using IC 7483. [10]

(*b*) Implement the following function using 4 : 1 MUX and logic gates : [6]

$$F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 15).$$

Or

6. (*a*) Draw and explain 4-bit BCD adder using IC 7483. Validate it with any *two* examples. [8]

(*b*) Design 16 : 1 Mux using 4 : 1 Mux (with enable inputs). Explain your circuit in short. [8]

SECTION II

7. (*a*) Design D Flip-Flop using T Flip-Flop. [4]

(*b*) Explain with a neat diagram working of Serial in Parallel out 4-bit shift register. Draw necessary timing diagrams. [6]

(*c*) Give any *four* applications of shift registers and describe in brief : [8]

(*i*) Ring Counter

(*ii*) Johnson Counter.

Or

8. (*a*) Explain with a neat diagram, working of 3-bit Up-down asynchronous counter. Draw necessary timing diagrams. [10]

(*b*) Design sequence detector using JK Flip-Flops to detect the following sequence ..... 111 ..... . [8]

9. (*a*) Draw ASM chart for the following state machine : "A two bit counter with output 'Q_1, Q_0' and enable signal 'X' is to be design. If 'X' = 0, Counter changes the state as '00—01—10—00'." If X = 1, Counter should remain in the present state. Design circuit using JK ff and suitable MUXs. [10]

(*b*) Write VHDL code and NAND gate. [6]

Or

10. (*a*) Describe different modeling styles of VHDL with suitable examples. [12]

(*b*) Write VHDL code for D Flip-Flop. [4]

11. (*a*) Draw and explain the general structure of PLA. [8]

(*b*) With neat block diagram explain microprocessor architecture. [8]

Or

12. (*a*) Design and explain PLD for 3 : 8 decoder. [8]

(*b*) Explain what is Bus ? Give different types of Bus used by a microprocessor. [4]

(*c*) Explain the function of the following : [4]

(*i*) ALU

(*ii*) Program Counter.