Total No. of Questions—**12**] [Total No. of Printed Pages—**4+2**

Seat No.	

S.E. (Computer Engineering) (Second Semester)

EXAMINATION, 2014

MICROPROCESSOR AND INTERFACING TECHNIQUES

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answers to the two sections should be written in separate answer-books.

(*ii*) Answer any *three* questions from each section.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right side indicate full marks.

(*v*) Use of calculator is allowed.

(*vi*) Assume suitable data if necessary.

SECTION I

1. (*a*) Draw and explain 8086 Internal Architecture in brief. [8]

(*b*) Explain the physical address formation in an 8086 microprocessor. [8]

P.T.O.

Or

2. (*a*) Draw and explain the write timing cycle of 8086 microprocessor in minimum mode. [8]

(*b*) State the difference between memory mapped I/O and I/O mapped I/O. [8]

3. (*a*) Explain the following addressing modes with *one* example each :

(*i*) Direct Addressing

(*ii*) Immediate Addressing

(*iii*) Base Register Addressing

(*iv*) Index Addressing. [8]

(*b*) Write an Assembly Language Program to generate a delay of 1 sec using a microprocessor running at 5 MHz. Also show the delay calculation. [8]

Or

4. (*a*) Write an Assembly Language Program to mask the lower nibble of an 8 bit number. Assume the 8 bit number is in the AL register. Write appropriate comments. [8]

(*b*) Determine the register contents of AL, BL and the six status after the following instruction are executed : [8]

```
STC

MOV  AL, 4CH

SBB   AL, 3EH

XOR   BL,  BL

MOV  [SI], BL
```

5. (*a*) State the difference between DOS calls and BIOS calls. [8]

(*b*) What is PSP ? Draw and explain the structure of PSP. [10]

Or

6. (*a*) What is TSR ? Explain the structure of TSR in detail. [10]

(*b*) Differentiate between .COM and .EXE files. [8]

SECTION II

7. (*a*) Draw and explain in brief the block diagram of 8255 PPI. [8]

(*b*) An 8251 is to be initialized as follows :

(*i*) 7 bits/character

(*ii*) Even parity

(*iii*) 1 stop bit

(*iv*) Baud rate factor × 64

(*v*) DTR and RTS asserted

(*vi*) Error flag reset.

Write the sequence of instructions required to initialize an 8251 at addresses 80 H and 81 H. [8]

Or

8. (*a*) Explain with diagram successive Approximation ADC. [8]

(*b*) Explain the working of LVDT with the help of a neat diagram. Also state the advantages and disadvantages of LVDT. [8]

9. (*a*) Draw and explain functional block diagram of 8279 keyboard and display Controller. [8]

(*b*) What are the different modes of operation of 8253 timer ? Explain mode 2 and mode 4 with waveforms. [8]

Or

10. (*a*) Draw and explain the following 8279 commands :

(*i*) Keyboard/display mode set command.

(*ii*) Read FIFO/sensor RAM command. [8]

(*b*) Explain the various data transfer modes of 8237/8257 in detail. [8]

11. (*a*) Draw and explain the minimum mode configuration of the 8086. [10]

(*b*) Explain the status word and control word of 8087 Numeric Co-processor. [8]

Or

12. Design a 8086 based system with the following specifications : [18]

(*i*) 8086 working at 10 MHz in maximum mode.

(*ii*) 32 KB EPROM using 16 KB devices.

(*iii*) 256 KB RAM using IC 62512. Clearly show the memory map.