Total No of Questions: [12] *SEAT NO. :*

[Total No. of Pages : 3]

S.E. 2008 (Information Technology)

Computer Organization(214442)

(Semester - I)

Time: 3 Hours *Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6 from section I and Q.7 or Q.8, Q.9 or Q.10, Q.11 or Q. 12 from section II.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right side indicate full marks.***
5) ***Use of Calculator is allowed.***
6) ***Assume Suitable data if necessary***

SECTION I

Q1)	a)	Compare restoring and non-restoring division algorithm. Divide the following numbers using non-restoring algorithm and justify your answer. Dividend = $(24)_{10}$, Divisor = $(7)_{10}$	[10]
	b)	Draw IEEE standard single precision and double precision floating point formats. Represent $(99.75)_{10}$ in single precision and double precision IEEE format.	[8]
		OR	
Q2)	a)	Draw flowchart of Booth's algorithm for signed multiplication. How does bit pair recoding technique achieve faster multiplication? Bit pair recode multipliers: $(110110101111001)_2$ and $(0101101010010101)_2$	[10]
	b)	Draw Von Neumann Architecture and explain function of registers in it.	[8]
Q3)	a)	State addressing modes for the following instructions and show physical address generation: (i)MOV [BP], AX (ii)MOV AX, [2000H] (iii)MOV CX, [BX][SI] (iv)MOV AX, [BX][SI+0020H]	[8]
	b)	Draw and explain programmer's model of 8086.	[8]
		OR	
Q4)	a)	Specify factors which decide instruction length. Draw and explain instruction format for INTEL processors.	[8]
	b)	Draw timing diagram for memory read cycle of 8086 and list operations in each T state.	[8]

Q5)	a)	Explain the control sequence needed to perform processor functions: (i) Fetching a word from memory (ii)Performing an arithmetic or logical operation.	[8]
	b)	Draw the diagram of microprogrammed control unit and give its advantages and disadvantages.	[8]
		OR	
Q6)	a)	Draw and explain single bus organization of the CPU, showing all the registers and data paths.	[8]
	b)	Explain the design of multiplier control unit using Delay Element Method.	[8]
		SECTION II	
Q7)	a)	What is MESI protocol? Explain the meaning of each of the four states of the MESI protocol.	[8]
	b)	Discuss direct mapping and set associative cache mapping techniques with respect to mapping function, address structure, merits and demerits.	[10]
		OR	
Q8)	a)	Write short note on (any 2) (i) RAID (ii)DVD (iii)SDRAM (iv)EEPROM	[8]
	b)	State the page replacement strategies and explain any three in detail with example.	[10]
Q9)	a)	Compare: (i)Memory Mapped I/O and I/O Mapped I/O (ii)Programmed I/O and Interrupt driven I/O	[8]
	b)	State features of 8251 and explain difference between synchronous and asynchronous serial communication.	[8]
		OR	
Q10)	a)	What is DMA? Explain demand transfer mode and block transfer mode of DMA data transfer.	[8]
	b)	Write short note on (any 2): (i)PCI (ii)SCSI (iii)USB ports	[8]
Q11)	a)	Compare closely coupled and loosely coupled multiprocessor configurations. Explain loosely coupled multiprocessor configuration.	[10]

	b)	What is cluster? State advantages of clustering.	[6]
		OR	
Q12)	a)	Write short notes on (any 4) (i)Superscalar architecture (ii)UMA (iii)NUMA (iv)RISC (v)CISC (vi)Instruction pipelining	[16]