(7)

Total No of Questions: [8] *SEAT NO. :*

[Total No. of Pages : 1]

S.E. 2012 (INFORMATION TECHNOLOGY)

DIGITAL ELECTRONICS & LOGIC DESIGN (214443)

(Semester - I)

Time: 2 Hours *Max. Marks : 50*

Instructions to the candidates:

1) *Answer Q.1 or Q.2 , Q.3 or Q.4 ,Q.5 or Q.6 and Q.7 or Q.8 .*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right side indicate full marks.*
4) *Assume Suitable data if necessary*

SECTION I

Q1)	a)	State conditions to be satisfied for interfacing, by driving & load gate. Draw and explain the interfacing of CMOS driving TTL	[6]
	b)	Minimize the following function using K-map and implement using basic logic gates $f(A,B,C,D) = \sum m(0,1,2,4,8,9,12,13) + d(3,6,7)$	[6]
		OR	
Q2)	a)	Convert the following Number into its equivalent Hexadecimal, Decimal & Binary Number (show step-by-step process of conversion): i. $(357.2)_8$ ii. $(458.54)_8$	[6]
	b)	Draw and explain the look ahead carry generator.	[6]
Q3)	a)	Explain the difference between asynchronous and synchronous counter & Convert J- K flip- flop into D-FF. Show the design.	[6]
	b)	Draw an ASM chart of 2 bit up - down counter having a mode control input.	[6]
		OR	
Q4)	a)	Draw and explain the behavior of M-S JK flip-flop with waveform.	[6]
	b)	Draw and explain Johnson counter with initial state "1110", from initial state explain all possible states.	[6]
Q5)	a)	Explain the difference between CPLD and FPGA.	[6]
	b)	What is meant by CPLD? Draw & Explain the block diagram of CPLD	[7]
		OR	
Q6)	a)	Give the comparison between PROM, PLA and PAL.	[6]
	b)	Design the full adder using PLA.	[7]
Q7)	a)	Explain with example Dataflow and behavioral modeling styles used in VHDL programming.	[6]
	b)	Explain with example 'signal 'and 'variable' in VHDL.	[7]
		OR	
Q8)	a)	Define entity declaration for AND gate. Also write architecture of AND gate in structural & Data modeling style.	[6]
	b)	What is the difference between behavioral model and structural model in VHDL?	[7]