Total No of Questions: [08] *SEAT NO. :*

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S.E. 2012 (INFORMATION TECHNOLOGY)
(214450) PROCESSOR ARCHITECTURE AND INTERFACING
(Semester - II)

Time: 2 Hours *Max. Marks : 50*

Instructions to the candidates:

1) *Answer Q.1 or Q.2 , Q.3 or Q.4 ,Q.5 or Q.6 and Q.7 or Q.8 .*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right side indicate full marks.*
4) *Assume Suitable data if necessary*

SECTION I

Q1) a) List and explain any three assembler directives used in 80386 programming. [6]

b) Explain pipelined bus cycles for READ operation with neat diagram [6]

OR

Q2) a) With respect to following points explain – Assembler, Linker and Debugger- [6]

1.Function 2.Input and Output 3.Command

b) Explain the significance of the following signals of the 80386. [6]

i) BE0# - BE3#

ii) PREQ

iii) NA#

Q3) a) What is TLB? With diagram explain role of TLB of 80386 [6]

b) How is I/O level protection achieved? Explain I/O permission bit map [6]

OR

Q4) a) What do you mean by dual core processor? List down the features of dual core processor. [6]

b) Explain how interrupts are handled in protected mode of 80386. [6]

Q5) a) Identify and justify addressing mode of the following 8051 instructions: [6]

i. MOVX A, @DPTR

ii. MOVC A, @A + PC

iii. MOV DPTR, #2550H

b) How many Register Banks does 8051 have? Explain with the help of diagram. How to change the current working register bank? [7]

OR

Q6) a) Explain the following instructions in 8051 : [6]
(i) MOV A, Rn
(ii) DIV AB
(iii) SWAP A

b) Draw and explain Architecture of 8051 Microcontroller. [7]

Q7) a) List operating modes of Timer of 8051 and explain any two of them. [7]

b) Explain the different types of interrupt in 8051. [6]

OR

Q8) a) For serial communication, what are the SFR's used in 8051? Explain in detail with its structure. [7]

b) Explain IE and IP SFR's of 8051 Microcontroller. [6]