Total No. of Questions : 12]

SEAT No. :

P3180

[Total No. of Pages :2

[4859]-219

B.E. (Computer) (Semester- II)

VLSI AND DIGITAL SYSTEM DESIGN

(2008 Pattern) (Elective-IV)

Time : 3 Hours] *[Maximum Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data if necessary.***

SECTION-I

Q1) a) Explain design methodology with flow chart for ASIC design. **[8]**

b) Explain the role of technology scaling in growth of IC Design. **[9]**

OR

Q2) a) Explain the need of layout design rules. Explain design rules for interconnects. **[9]**

b) Explain the classification of IC technology based on circuit technology. **[8]**

Q3) a) Explain Shallow Trench Isolation (STI) with process flow. **[8]**

b) Explain limitations of further scaling of CMOS device. **[9]**

OR

Q4) a) Explain geometry parameters of interconnects. Explain merits and demerits of Cu interconnects over AI interconnect. **[8]**

b) Explain the device isolation in details. **[9]**

Q5) a) Explain basic properties of Silicon Wafer. **[4]**

b) Explain steps in active region formation. **[4]**

c) Explain Chemical vapor oxidation technique. **[8]**

OR

Q6) a) Write a short note on **[8]**

i) Czochrlski and Float-Zone Crystal Growth Methods

ii) Mask engineering

P.T.O.

b) Explain photolithography process in detail. **[8]**

SECTION-II

Q7) a) Explain merits and demerits of FPGA over ASIC. **[8]**

b) Compare data flow, behavioral and structural modeling styles. **[9]**

OR

Q8) a) Explain the following terms with examples. **[9]**

i) Concurrent statements

ii) Variable

iii) Entity

b) Write VHDL Code for **[8]**

i) 8:1 Multiplexer.

ii) D-Flip flop

Q9) a) Explain the PAL and PLA in details. **[8]**

b) Explain static and dynamic circuit design styles. **[8]**

OR

Q10)a) Explain static and dynamic behavior of CMOS devices and Circuits. **[8]**

b) Explain different digital design levels. **[8]**

Q11)a) Explain the metastability in details. **[5]**

b) Explain software aspects of digital design. **[8]**

c) Discuss logic levels and noise margins with respect to CMOS circuits. **[4]**

OR

Q12)a) Draw a neat diagram and explain briefly 6-T SRAM. **[8]**

b) For Combinational Logic design explains the following design metrics. **[9]**

i) Power Consumption

ii) Propagation Delay

iii) Noise margin

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