Total No. of Questions : 12]

SEAT No. :

P1755

[Total No. of Pages : 3

[4859]-113
B.E. (Electronics Engineering)
VLSI DESIGN
(2008 Course) (Semester - I)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer 3 questions from section I and 3 questions from section II.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Use of logarithmic tables slide rule, Mollier charts, electronic pocket calculator and steams tables is allowed.***
6) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explain CMOS inverter and its transfer characteristics in detail. How to achieve symmetry in these characteristics. **[8]**

b) Design 4:1 Mux using transmission Gates. Compare it with conventional methods. **[8]**

OR

Q2) a) Explain the followings: **[8]**

i) Hot electron effect

ii) Body effect

b) Explain the static & dynamic power dissipation. Derive an expression for power delay product. **[8]**

Q3) a) Explain DRAM in detail with suitable diagram. **[8]**

b) Give the classification of memory with the application in each case. **[8]**

OR

P.T.O.

Q4) a) Differentiate between SRAM & DRAM technologies. **[8]**

b) Explain read/write operation of 6T SRAM cell with the help of timing diagrams. **[8]**

Q5) a) Explain different modeling styles in VHDL coding with examples. **[9]**

b) Compare VHDL **[9]**

i) Variables and Signals.

ii) Synthesizable and Non-synthesizable statements.

OR

Q6) a) Differentiate Moore and Mealy machine with suitable examples. **[9]**

b) Write a VHDL code for a JK FF. Also write a test bench for it. **[9]**

SECTION - II

Q7) a) Draw block diagram of CPLD and List its Specifications. **[8]**

b) Differentiate between FPGA & CPLD. **[8]**

OR

Q8) Explain:

a) Antifuse **[5]**

b) CLB **[6]**

c) Specification of FPGA **[5]**

Q9) a) Explain with Block Diagram of Full & Partial Scan. **[10]**

b) Explain stuck at fault model. **[8]**

OR

Q10) Write Short Notes on: **[18]**

a) DFT

b) JTAG

c) BIST

d) TAP Controller

Q11)a) Explain Global and Switch box routing. **[8]**

b) Explain off chip connection and I/O Architecture. **[8]**

OR

Q12) Write short notes on the following: **[16]**

a) Power distribution and optimization.

b) Two Phase clocking and clock distribution.