Total No. of Questions : 10]

SEAT No. :

P1868

[Total No. of Pages :3

[4859]-1054
B.E. (Electronics)
DSP PROCESSORS
(2012 Pattern) (Semester - I) (404205A) (Elective-II)

Time : $2\frac{1}{2}$ *Hours]* *[Max. Marks : 70*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4,Q.5 or Q.6,Q7 or Q.8, Q9 or Q.10.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicates full marks.***
4) ***Assume suitable data if necessary.***

Q1) a) Explain the Fixed point and Floating point number format. What are the criteria for selecting the number format to be used while designing the DSP based system? **[4]**

b) For the IIR filter, determine $H(z) = \frac{z-1}{(z-0.25)(z-0.5)}$ **[6]**

i) Frequency response function

ii) Impulse response

iii) Step response

OR

Q2) a) What is the need of shifter used in DSP architecture? Explain with suitable cases. **[5]**

b) What distinguishes a digital signal processor from a general purpose microprocessor with regard to basic capabilities? Explain. **[5]**

Q3) a) What is meant by overflow and underflow in an arithmetic computation? How is an overflow condition detected? **[5]**

b) Explain the barrel shifter used in DSP architecture with suitable diagram. **[5]**

OR

P.T.O.

Q4) a) What is DFT and FFT? Which is computationally efficient? Explain with suitable Numerical values. **[5]**

b) What are the various addressing modes used in DSP implementation? Explain any two with suitable example. **[5]**

Q5) a) What are the characteristics of FIR filter? Explain its implementation using block diagram. **[8]**

b) Explain the Q-notations used in DSP algorithm implementation? **[3]**

c) What is an Adaptive filter? Explain the implementation of adaptive filter with suitable diagram and mathematical equation? **[6]**

OR

Q6) a) Explain the implementation of IIR filter using suitable diagram and mathematical equation? **[8]**

b) What are the values represented by the 16-bit fixed point number N=4000h in the Q15 and Q7 notations? **[4]**

c) Explain the implementation of 2-D signal processing operations in DSP architecture. **[5]**

Q7) a) Determine the following for a 128-point FFT computations? **[6]**

i) Number of stages

ii) Number of butterflies in stage

iii) Number of butterflies needed for the entire computation.

b) Explain the implementation 8 point DIT FFT algorithm using signal flow graph and number of arithmetical computation involved. **[11]**

OR

Q8) a) If number of data points available in input seqeuence is 7 then. **[4]**

i) What is the length of FFT you will select for computation? Why?

ii) What happens if length of FFT is more than sufficient?

b) What is the need of scaling in FFT computation? What happens if scaling is not proper? **[5]**

c) A time domain sequence of 73 elements is to be convolved with another time-domain sequence of 50 elements using DFT-IDFT, method. To implement DFT-IDFT, DIT-FFT algorithm is to be used. Determine the total number of complex multiplications needed to implement the convolution. Assume that each butterfly computation requires one complex multiplication. **[8]**

Q9) a) What is DMA? Explain its operation with suitaple example. **[8]**

b) Explain the following in context with DSP. **[8]**

i) Multichannel Buffered Serial Port (McBSP)

ii) CODEC

OR

Q10)a) What is an interrupt? Explain the handling of interrupts by the DSP processor? **[8]**

b) Explain the programmed I/O interface with suitable example? **[8]**