

Total No. of Questions : 10]

SEAT No. :

P1970

[Total No. of Pages : 2

[4859]-1047

B.E. (Electronics Engg.) (End Semester)

VLSI DESIGN

(2012 Pattern)

Time : 3 Hours]

[Max. Marks : 70

Instructions to the candidates:

- 1) Neat diagrams must be drawn wherever necessary.*
- 2) Figures to the right indicate full marks.*
- 3) Use of logarithmic tables slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.*
- 4) Assume suitable data, if necessary.*

- Q1)** a) What is feature size and λ ? List basic λ rules in CMOS design? [6]
b) Write short note on velocity saturation. [4]

OR

- Q2)** a) Derive the expression for Dynamic power dissipation. [5]
b) Draw block diagram and explain architecture of FPGA. [5]

- Q3)** a) Write a VHDL code for BCD to seven segment Decoder. [5]
b) Explain Noise margin. Give its expressions. [5]

OR

- Q4)** a) Explain various attributes in VHDL with suitable examples. [5]
b) What is metastability? How can it be removed? [5]

- Q5)** a) Compare SRAM and DRAM. List various types of memories. [8]
b) Draw any 2 schematics of DRAM cells. Explain Write and Read operation of any one of them. [8]

OR

- Q6)** a) Draw and explain the schematic of SRAM cell with necessary peripherals. [8]
b) Write short note on : [8]
i) Refresh circuit
ii) Sense amplifier

P.T.O.

- Q7)** a) What are challenges in routing? Explain switch box routing. [8]
b) Explain floor planning, its purposes and the rules. [8]

OR

- Q8)** a) What is Global routing. Explain Maze and line probe routing algorithms in detail. [8]
b) Explain Power distribution and power optimization in details. [8]

- Q9)** a) What are stuck open, stuck short faults? Also explain stuck at 1 and stuck at 0 faults with example. [9]
b) What is Built in self test? Explain BIST for RAM. [9]

OR

- Q10)** a) What is need of Boundary scan? Explain Boundary scan technique in detail. [6]
b) What is necessity of DFT. [4]
c) What is Test access port? Explain TAP controller with help of state machine. [8]

