Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

Seat No.	

[4857]-203

S.E. (Computer/IT) (First Semester) EXAMINATION, 2015
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. **:—** (*i*) Answers to the *two* Sections should be written in separate answer-books.

(*ii*) Answer any *three* questions from each Section.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Use of calculator is allowed.

(*vi*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Express the following numbers in binary, show the step-by-step equations and calculations : [6]

(*i*) $(110.110)_{10}$

(*ii*) $(234.234)_{10}$.

(*b*) Convert 4-bit Gray Code into corresponding BCD code. Show truth table and MSI circuit. [6]

(*c*) Perform the following Hexadecimal subtraction and show the answer in Hexadecimal only : [6]

(*i*) $(ABC)_{16} - (CBA)_{16}$

(*ii*) $(759)_{16} - (957)_{16}$.

P.T.O.

Or

2. (*a*) Convert the following octal numbers into its equivalent decimal and hex : [6]

(*i*) $(555)_8$

(*ii*) $(777)_8$.

(*b*) Solve the following equations using K-map minimization technique : [12]

(*i*) $Z = f(A, B, C, D) = \pi(2, 7, 8, 10, 11, 13, 15)$

(*ii*) $Z = f(A, B, C, D) = \Sigma(0, 3, 4, 9, 10, 12, 14)$.

3. (*a*) Draw 3-i/p standard TTL NAND gate with Totem pole. Explain operation of transistor (ON/OFF) with suitable input conditions and truth table. [10]

(*b*) What is logic family ? Explain types of logic families in detail. [6]

Or

4. (*a*) With the help of Quine-McClusky technique determine the PI, EPI for the following equation : [10]

$Z = f(A, B, C, D) = \Sigma(0, 3, 8, 9, 10, 12, 15)$.

(*b*) Explain standard TTL characteristics in brief. [6]

5. (*a*) Design BCD to 7-segment code decoder using logical gates. Assume common Anode 7-segment LED's. [8]

(*b*) Design 16 : 1 mux using 4 : 1 mux (with enable inputs). Explain your circuit in short. [8]

Or

6. (*a*) Draw and explain 4-bit BCD adder using IC 7483. Explain any *two* BCD addition operations. [10]

(*b*) Design BCD to 7-segment code decoder using logical gates. Assume common Cathode 7-segment LED's. [6]

SECTION II

7. (*a*) Explain with a neat diagram, working of 3-bit Up-Down Synchronous counter. Draw necessary timing diagrams. [10]

(*b*) Design a sequence generator with a sequence 1101011. [8]

Or

8. (*a*) Design SR Flip-Flop using JK Flip-Flop. [4]

(*b*) Explain with a neat diagram working of Parallel In Serial Out 4-Bit shift register. Draw necessary timing diagrams. [6]

(*c*) Give any *four* applications of Shift Registers. Also explain 4-bit Johnson's counter. [8]

9. (*a*) Describe architectural blocks of FPGA. Briefly explain function of each. [10]

(*b*) Write VHDL code for 4 : 1 mux. [6]

Or

10. (*a*) With the help of an ASM chart, design a modulo 6 Up-Down counter. [10]

(*b*) Write VHDL code for D Flip Flop. [6]

11. (*a*) Draw and explain general structure of PLA. [8]

(*b*) Explain what is Bus ? Give different types of Bus used by a microprocessor. Explain the function of :

(*i*) ALU

(*ii*) Program Counter. [4]

Or

12. (*a*) Design Using PLD a 3 : 8 Decoder. [8]

(*b*) Draw a generalized block diagram of a microprocessor. Briefly explain function of each block. [8]