Seat	
No.	

[4857]-1075

S.E. (Computer Engineering) (First Semester)

EXAMINATION, 2015

MICROPROCESSOR ARCHITECTURE

(2012 **PATTERN**)

Time: Two Hours

Maximum Marks: 50

- **N.B.** :— (i) Answer any four questions 1 or 2, 3 or 4, 5 or 6 and 7 or 8.
 - (ii) Neat diagrams must be drawn wherever necessary.
 - (iii) Figures to the right indicate full marks.
- 1. (a) Explain registers available in 8086 microprocessor. [3]
 - (b) Explain how physical address is formed in 80386 Dx microprocessor. [6]
 - (c) Explain the following signal function of 80386 Dx microprocessor: [3]
 - (1) Lock #
 - (2) BE0 # BE3 #
 - (3) HOLD and HLDD.

2.	(a)	Explain four level of hierarchical protection in 80386	Dx
		microprocessor.	[3]
	(<i>b</i>)	Draw and explain the architecture of 8086 microprocessor.	[6]
	(c)	What is maximum size of each segment in 80386	Dx
		microprocessor ? Why ?	[3]
3.	(a)	Explain non-pipelined read cycle with timing diagram.	[5]
	(<i>b</i>)	List and explain iteration control instructions of 80386	Dx
		microprocessor.	[4]
	(c)	Briefly explain how to set V86 mode	[3]
		Or	
4.	(a)	Explain four different processor control instructions.	[4]
	(<i>b</i>)	Explain non-pipelined write cycle with timing diagram.	[5]
	(c)	Briefly explain how to be protected mode.	[3]
5.	(a)	What is multicore architecture ? Explain.	[3]
	(<i>b</i>)	Explain the execution model of SIMD with neat diagram.	[6]
	(c)	Explain software developer's viewpoint about multic	ore
		processor.	[4]

6.	(<i>a</i>)	Write different advantages of multicore design.	[3]
	(<i>b</i>)	Explain different multiprocessor architectures.	[6]
	(c)	What is front side bus, back side bus? Explain.	[4]
7.	(a)	Explain different instruction sets for I-A-64 architecture.	
	(<i>b</i>)	Explain Intel Hyperthreading Technology.	[4]
	(c)	What are the differences between IA-32 basic execut	tion
		environment and 64 bit mode execution environment ?	[3]
		Or	
8.	(a)	Explain X86 virtualization technology in detail.	[6]
	(<i>b</i>)	Explain data types of 64 bit architecture.	[4]
	(c)	Enlist features of SSE.	[3]