Total No. of Questions : 12]

SEAT No. :

P1460

[Total No. of Pages :4

[4759] - 217
B.E. (Computer)
ADVANCED COMPUTER ARCHITECTURE
(2008 Pattern) (410449) (Semester - II)

Time :3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer to the two Sections should be written in separate answer books..***
2) ***Answer any three questions from each section.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explain in brief general classification of multiprocessor based on following techniques. **[12]**

i) Degree of coupling

ii) Memory access

iii) Flynn's classification

iv) Feng's classification

b) Explain Implicit and Explicit parallelism. **[6]**

OR

Q2) a) What is scalable computer system? Explain various parameters affecting scalability of computer system. **[10]**

b) State and explain features of Itanium Architecture for software pipelining support. **[8]**

Q3) a) Design a six bit multiplier using CSA Tree. How it can be viewed as k-stage arithmatic pipeline? With same Hardware how an n-bit multiplier can be designed? Assuming single clock cycle per processing stage, find the total No. of clock cycles for the same. **[10]**

b) Discuss the various features of SPARC Architecture. **[6]**

OR

P.T.O.

Q4) a) Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I_1, I_2, I_3, I_4 in stages S_1, S_2, S_3, S_4 are as shown below **[8]**

	S_1	S_2	S_3	S_4
I_1	2	1	1	1
I_2	1	3	2	2
I_3	2	1	1	3
I_4	1	2	2	2

Calculate total number of cycles needed to execute the following loop

for (i = 1 to 2)

{

I_1;

I_2;

I_3;

I_4;

}

Also draw the space time diagram showing execution of all instructions through successive pipeline stages.

b) Identify All of the RAW, WAR and control Hazards in following instruction sequence. **[8]**

DN r_2, r_5, r_8

SUB r_9, r_2, r_7

ASH r_5, r_{14}, r_6

MUL r_{11}, r_9, r_5

BEQ r_{10}, #0, r_{12}

OR r_8, r_{15}, r_2

Q5) a) With suitable examples, explain the necessity of data Routing in array processors. **[8]**

b) Discuss a problem of 3×3 matrix multiplication on a mesh network. Obtain it's time complexity. **[8]**

OR

Q6) a) Explain the programming model of cray-1 vector Architecture. **[8]**

b) What is use of data Routing functions? With examples discuss the necessity of data routing in array processors. **[8]**

SECTION- II

Q7) a) Explain following bus arbitration algorithms in brief. **[9]**

i) RDC

ii) FCFS

iii) Polling

b) Discuss COWs and NOW's architecture with suitable block diagrams. **[9]**

OR

Q8) a) Explain with typical cluster computing Architecture the various operating system issues to be handled in the design of cluster computing system. **[9]**

b) What are different Multiprocessors Architectures? What are Network and software factors limiting performances of these systems? **[9]**

Q9) a) With suitable examples explain shared memory parallel programming. What is SPMD programming? **[8]**

b) Explain with examples the use of synchronization primitives in parallel programming. **[8]**

OR

Q10)a) With standard constructs and features explain how parallelism is achieved in data parallel programming? **[8]**

b) Explain use of following primitives used in parallel programming. **[8]**

i) Send ( )

ii) Receive ( )

iii) Fork ( )

iv) Join ( )

Q11)a) With suitable example explain how parallel algorithms are written for multiprocessor systems. **[8]**

b) Explain in detail the steps usually followed for generating a multiprocessing application from a sequential application. **[8]**

OR

Q12)a) Explain the classification of parallel algorithms with suitable examples. **[8]**

b) How parallel virtual machine acts as a programming interface for parallel processing? **[8]**

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