Total No. of Questions : 12]

SEAT No. :

P1465

[Total No. of Pages :3

[4759] - 222
B.E. (Computer)
VLSI & DIGITAL SYSTEMS DESIGN
(2008 Pattern) (Semester - II) (Elective - IV)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data. if necessary.***

SECTION - I

Q1) a) Compare Speed-Power Performance of available technologies. **[8]**

b) Explain the types of technology scaling. **[9]**

OR

Q2) a) Explain the layout design rules for devices and interconnects. **[9]**

b) Explain the classification of IC technology based on design style. **[8]**

Q3) a) Explain Shallow Trench Isolation (STI) with process flow. **[8]**

b) Explain fabrication process for CMOS device. **[9]**

OR

Q4) a) Explain fabrication of Cu interconnects with suitable diagram. **[8]**

b) Write a short note on **[9]**

i) Gate formation

ii) Contact formation

iii) Source drain region formation

P.T.O.

Q5) a) Explain basic properties of Silicon Wafer. **[4]**

b) Explain purification steps of raw silicon wafer. **[4]**

c) Explain Chemical vapor oxidation technique. **[8]**

OR

Q6) a) Write a short note on **[8]**

i) Optical Lithography

ii) Thermal Oxidation

b) Explain wet etching and plasma etching. **[8]**

SECTION - II

Q7) a) Explain Island style and Row based FPGA architectures in detail. **[8]**

b) Explain different Modeling styles in HDL. **[9]**

OR

Q8) a) Explain the following terms with examples. **[9]**

i) Identifier

ii) Variable

iii) Array

b) Write VHDL Code for Lift Controller. **[8]**

Q9) a) Explain the types of programmable logic devices in details. **[8]**

b) Explain Application Specific IC's Design Flow. **[4]**

c) Explain CMOS inverter with VTC. **[4]**

OR

Q10)a) Explain static and dynamic behavior of CMOS devices and Circuits. **[8]**

b) Explain role of software tools in digital design. Explain the types of software tools in VLSI design. **[8]**

Q11)a) Explain the metastability in details. **[5]**

b) List out different steps for designing Clocked synchronous state machine. **[8]**

c) Explain merits and demerits of CPLD. **[4]**

OR

Q12)a) Explain timing parameters for Read and Write Operation in Static RAM. **[8]**

b) For Combinational Logic design explains the following. **[9]**

i) Timing diagram

ii) Propagation Delay

iii) Timing specification

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