Total No. of Questions : 12]

SEAT No. :

P1408

[Total No. of Pages :3

[4759] - 117
B.E. (Electronics)
ADVANCED COMPUTER ARCHITECTURE
(2008 Course) (Semester -I) (Elective - II) (404205)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer any three questions from each section.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data if necessary.***

SECTION - I

Q1) a) Discuss Flynn's classification of parallel computer in detail. **[8]**

b) Explain Handler's classification. **[8]**

c) What is cluster computing? **[2]**

OR

Q2) a) Discuss in detail the application of parallel processing in **[12]**

i) Predictive modelling and simulation

ii) Engineering design and automation

b) Discuss and explain instruction level parallelism and Thread level parallelism. **[6]**

Q3) a) Consider the following pipeline reservation table **[10]**

Clock cycles → / States ↓	0	1	2	3	4	5	6
S_1	X		X				X
S_2				X		X	
S_3			X		X		

i) Determine latencies in the forbidden list F and collision vector C.

P.T.O.

ii) Draw the state transition diagram.

iii) List all simple cycles and greedy cycles.

iv) Determine minimum average latency (MAL).

v) For a pipelink clock period τ = 20ns. Determine maximum throughput of the pipeline.

b) Explain the 'Internal Forwarding Techniques'. **[6]**

OR

Q4) a) Explain with suitable examples the various types of hazards in a pipeline processor. How these hazards can be resolved? **[8]**

b) Explain the static & dynamic branch prediction techniques used in a pipeline processor. **[8]**

Q5) a) State the characteristics of CRAY-1 computer system. Draw and explain the computation section of CRAY-1 vector processor. **[12]**

b) Explain pipeline chaining. **[4]**

OR

Q6) a) Explain four types of vector instructions. **[8]**

b) What are vector processors? Discuss two different architectural configurations of vector processor. **[8]**

SECTION - II

Q7) a) Explain static and dynamic network topologies used in interconnection networks with proper examples. **[10]**

b) Explain matrix multiplication on SIMD architecture. **[8]**

OR

Q8) a) Explain the algorithm to compute Fast Fourier Transform for SIMD architecture. **[10]**

b) Explain the cube interconnection network and hypercube interconnection network. **[8]**

Q9) a) Give the typical architecture of MPP. Explain in detail. **[8]**

b) Write short note on: **[8]**

i) Cross bar switch

ii) Multiport memory

OR

Q10)a) Explain processor characteristics of multiprocessor. **[8]**

b) Explain the architecture of IBM 4 processor. **[8]**

Q11)a) What is latency hiding techniques with respect to multithreaded architecture. Elaborate any two techniques. **[8]**

b) Explain the following terms associated with message passing: Synchronous and asynchronous. **[8]**

OR

Q12)a) State the following terms with respect to multithreading **[8]**

i) Latency

ii) Number of threads

iii) Context-switching overhead

iv) Interval between switches

b) What is data parallel programming. Explain in detail. **[8]**

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