Total No. of Questions : 12]		SEAT No.:
P1414	[4759]-130	[Total No. of Pages : 2

## **B.E.** (Electronics)

## NANOTECHNOLOGY IN ELECTRONICS

(2008Course) (Elective-IV) (Semester-II)

Time: 3 Hours] [Max. Marks: 100 Instructions to the candidates: Answers to the two sections should be written in separate answer books. 2) Neat diagrams must be drawn wherever necessary. Figures to the right side indicate full marks. 3) Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q,7 or Q.8, Q.9 or Q.10 and Q.11 or 4) Q.12. Assume Suitable data if necessary. *5*) **SECTION-I** *Q1*) a) Explain any four tools used for making Nanostructures. [8] List out the limitations of semiconductor technology in the context of b) [8] nanostructures. OR Explain optical properties of semiconducting nanoparticles. **Q2)** a) [8] Explain molecular modeling of Nanoparticles. [8] b) *Q3*) a) Explain the principle of single electron transistor device. [8] Explain silicon Nanocrystal Non-volatile memory bit cell. [8] b) OR Draw and explain the process flow for integrating nanocrystal memory **Q4**) a) with standard CMOS technology. [8] Explain different nano CMOS devices with their application. b) [8] **Q5**) a) Explain with schematic apparatus to make metal nanoparticles. [9] Explain applications and properties of carbon Nanotube. [9] b) OR

[9]
application
EMS. [10]
o-machines hile design [ <b>10</b> ]
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al for future [8]
o- materials [ <b>8</b> ]
[16]
ising nano [ <b>8</b> ]
[8]