Total No. of Questions : 12]

SEAT No. :

P1406

[Total No. of Pages : 3

[4759] - 111
B.E. (Electronics Engineering)
VLSI DESIGN
(2008 Pattern) (Semester -I)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6 from Section-I & Q.7 or Q.8, Q.9 or Q.10, Q.11 or Q.12 from Section - II.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right side indicate full marks.***
5) ***Use of calculator is allowed.***
6) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explain CMOS inverter and its transfer characteristics in detail. How to achieve symmetry in these characteristics. **[8]**

b) Design 4:1 Mux using transmission Gates. Compare it with conventional methods. **[8]**

OR

Q2) a) Explain the following: **[8]**

i) Hot electron effect

ii) Body effect

b) Explain the static & dynamic power dissipation. Derive an expression for power delay product. **[8]**

Q3) a) Explain DRAM in detail with suitable diagram. **[8]**

b) Give the classification of memory with the application in each case. **[8]**

OR

Q4) a) Differentiate between SRAM & DRAM technologies. **[8]**

b) Explain read/write operation of 6T SRAM cell with the help of timing diagrams. **[8]**

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Q5) a) Explain different modeling styles in VHDL coding with examples. **[9]**

b) Compare in VHDL **[9]**

i) Variables and Signals

ii) Synthesizable and Non-synthesizable statements

OR

Q6) a) Differentiate Moore and Mealy machine with suitable examples. **[9]**

b) Write a VHDL code for a JK FF. Also write a test bench for it. **[9]**

SECTION - II

Q7) a) Explain in detail the classification of ASIC in detail. **[8]**

b) Draw & explain CMOS architecture of SRAM. **[8]**

OR

Q8) a) Explain the term **[8]**

i) CLB

ii) LUT

iii) IOB

iv) Switch Matric

b) With neat schematic explain the architectural building blocks of CPLD. **[8]**

Q9) a) Explain DFT in detail. How it can be categorized? Where it is useful. **[8]**

b) What is full scan and partial scan? Explain in detail. **[8]**

OR

Q10)a) Write a short note on: BIST, JTAG and TAP controller. **[8]**

b) What are the types of fault? Explain with schematic. **[8]**

Q11)a) What is power optimization? Explain the methods of optimization at various levels. **[9]**

b) Explain the following terms: **[9]**

i) Switch Box Routing

ii) Power distribution

iii) Global Routing

OR

Q12)a) Explain input pad, output pad and 3 stage pad design in a chip. **[9]**

b) What is clock skew and clock jitter? Explain different techniques of clock distribution. **[9]**

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