Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

| Seat No. | |
|---|---|

# [4757]-183

## S.E. (Computer/IT) (First Semester) EXAMINATION, 2015

## DIGITAL ELECTRONICS AND LOGIC DESIGN

## (2008 PATTERN)

**Time : Three Hours** **Maximum Marks : 100**

***N.B.*** :— (*i*) Answers to the two Sections should be written in separate answer-books.

(*ii*) Answer any *three* questions from each Section.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Use of calculator is allowed.

(*vi*) Assume suitable data, if necessary.

## SECTION I

**1.** (*a*) Convert the following decimal numbers into their equivalent binary, hexadecimal and octal numbers : [12]

(*i*) 936

(*ii*) 1507

(*iii*) 23.56

(*iv*) 1.025.

(*b*) Perform the following operations without converting the numbers to decimal : [6]

(*i*) $(1011)_2 \times (101)_2$

(*ii*) $(1000001)_2 \div (1101)_2$

P.T.O.

*Or*

**2.** (*a*) Express the following numbers in binary format. Write step by step solution : [6]

(*i*) $(762)_{\text{octal}}$

(*ii*) $(246)_{\text{decimal}}$

(*iii*) $(1101.11)_{\text{decimal}}$.

(*b*) Solve the following equations using corresponding minimization techniques : [12]

(*i*) $Z = f(A, B, C, D) = \pi(2, 7, 8, 10, 11, 13, 15)$

(*ii*) $Z = f(A, B, C, D) = \Sigma(0, 3, 4, 9, 10, 12, 14)$.

**3.** (*a*) Solve by Quine-McClusky technique : [10]

$Z = f(A, B, C, D) = \Sigma(0, 1, 3, 4, 6, 8, 10, 12, 14)$.

(*b*) Explain standard TTL characteristics in brief. [6]

*Or*

**4.** (*a*) Draw 2-i/p standard TTL NAND gate with Totem Pole. Explain operation of transistor (ON/OFF) with suitable input conditions and truth table. [8]

(*b*) Compare TTL and CMOS logic family (any 4 points). Also draw CMOS-NOR gate. [8]

**5.** (*a*) Design and implement 4-bit binary to gray code converter using basic gates. [8]

(*b*) Draw 4-bit BCD Adder by using IC 7483 and logic gates. [8]

*Or*

**6.** (*a*) Design 12 : 1 mux using 4 : 1 multiplexers (with enable inputs). Explain the truth table of your circuit in short. [8]

(*b*) Implement the following function using 4 : 1 MUX and logic gates : [8]

$$F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 15).$$

## SECTION II

**7.** (*a*) What is MOD counter ? Explain MOD-27 counter using IC 7490. Draw design for the same. [8]

(*b*) What is the difference between Asynchronous and Synchronous Counter ? Draw a 3-bit Asynchronous counter. Explain timing diagram for the same. [10]

*Or*

**8.** (*a*) Explain the difference between combinational and sequential circuit. Also convert J-K flip-flop into D-F/F and T-F/F. Show the Truth Table. [10]

(*b*) Give any *four* applications of Shift Registers. Also explain 4-Bit Johnson's Counter. [8]

**9.** (*a*) What is ASM chart ? Give its application and explain the MUX controller method with the suitable example. [8]

(*b*) What is VHDL ? Explain entity architecture declaration for 2-Bit X-NOR gate. [8]

*Or*

**10.** A sequential circuit has to count up from 111 to 000. The ckt also has i/p X. If X = 0, then circuit will count DOWN and if X = 1, then they will remain in the current state. Draw an ASM chart and state table for this circuit and design the circuit to generate the o/p using MUX controller method. [16]

**11.** (*a*) Explain basic characteristics of FPGA. [8]

(*b*) What is the difference between CPLD and FPGA. [8]

*Or*

**12.** (*a*) Explain in brief, the working of Address bus, Data bus and Control bus by assuming a basic operation. [8]

(*b*) Explain basic microprocessor architecture. [8]