Total No. of Questions—**12**] [Total No. of Printed Pages—**4+1**

Seat No.	

[4757]-192

S.E. (IT) (First Sem.) EXAMINATION, 2015

COMPUTER ORGANIZATION

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Solve Q. No. **1** *or* Q. No. **2,** Q. No. **3** *or* Q. No. **4** and Q. No. **5** *or* Q. No. **6** from Section I and solve Q. No. **7** *or* Q. No. **8,** Q. No. **9** *or* Q. No. **10** and Q. No. **11** *or* Q. No. **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Compare Restoring and Non-restoring division algorithm. Perform the division using restoring division algorithm : [10]

Dividend = 17, Divisor = 3.

P.T.O.

(*b*) Draw IEEE standards for single precision and double precision floating point numbers. Represent $(-84.25)_{10}$ in single precision and double precision format. [8]

Or

2. (*a*) Explain Booth's algorithm for signed multiplication. Multiply the following numbers using Booth's algorithm : [10]

A = 15 multiplicand

B = – 6 multiplier.

(*b*) Draw IAS (Von Neumann) Architecture and explain function of registers in it. [8]

3. (*a*) What do you mean by programmers model of 8086 ? Explain the same with neat diagram. [8]

(*b*) Describe the following addressing modes of 8086 along with suitable examples : [8]

(*i*) Immediate

(*ii*) Register indirect

(*iii*) Autoincrement

(*iv*) Index addressing mode.

Or

4. (*a*) Draw timing diagram for memory write cycle of 8086 in Minimum Mode and list operations in each T state. [8]

(*b*) State design factors in design of Instruction format. Draw instruction format for INTEL processor and explain various fields in it. [8]

5. (*a*) Draw and explain single bus organization of the CPU, showing all the registers and data paths. [8]

(*b*) Explain design of multiplier control unit using delay element method. [8]

Or

6. (*a*) Write control sequence for execution of the instruction ADD(R1), R2 for single bus architecture. [8]

(*b*) Compare : [8]

(*i*) Horizontal and vertical microinstruction representation.

(*ii*) Hardwired and microprogammed control unit.

SECTION II

7. (*a*) Explain the following terms : [8]

(*i*) Cache updation policies

(*ii*) Cache Hit and Cache miss.

(*b*) State cache mapping techniques ? Explain any *one* with neat diagram. [10]

Or

8. (*a*) What is Virtual memory ? Explain address translation mechanism for converting virtual address into physical address with neat diagram. [10]

(*b*) Write short notes on (any *two*) : [8]

(*i*) SDRAM

(*ii*) Optical Disk

(*iii*) RAID

(*iv*) EEPROM.

9. (*a*) Compare and explain programmed I/O and Interrupt driven I/O. [8]

(*b*) Write short notes on keyboard and scanner. [8]

Or

10. (*a*) Explain functions and features of IC 8255 and 8251. [8]

(*b*) Explain the working principle of the following : [8]

(*i*) Laser Printer

(*ii*) Video displays.

11. (*a*) Draw and explain loosely coupled multiprocessor configuration with its merits. [8]

(*b*) Explain briefly : [8]

(*i*) Instruction pipelining

(*ii*) Superscalar architecture.

Or

12. (*a*) Compare the following : [8]

(*i*) RISC and CISC

(*ii*) UMA and NUMA.

(*b*) What is cluster ? What are advantages of clustering ? Explain cluster classification. [8]