Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

Seat No.	

[4757]-198

S.E. (Information Technology) (Second Semester)

EXAMINATION, 2015

PROCESSOR ARCHITECTURE AND INTERFACING

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6** from Section I and Q. No. **7** *or* Q. No. **8**, Q. No. **9** *or* Q. No. **10**, Q. No. **11** *or* Q. No. **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right side indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Draw and explain 80386 real mode programmers model. [10]

P.T.O.

(*b*) Explain significance of the following signals of 80386 : [8]

(*i*) NA'

(*ii*) LOCK'

(*iii*) ADS'

(*iv*) BS16'

Or

2. (*a*) Draw timing diagram of address pipelined and non-pipelined read machine cycle for 80386 and list activities carried out in sequence. [10]

(*b*) Explain memory segmentation of 80386 microprocessor in real mode. [8]

3. (*a*) Compare and contrast : [8]

(*i*) .COM & .EXE programs

(*ii*) MACRO & PROCEDURE

(*b*) Explain the significance of the following assembler directives : [8]

(*i*) PUBLIC

(*ii*) DW

(*iii*) .STACK

(*iv*) EVEN

Or

4. (*a*) Explain any *four* addressing modes of 80386 showing physical address generation with example. [8]

(*b*) Draw and explain control word format for I/O and BSR mode of 8255. [8]

5. (*a*) How 80386 processor translates logical address into linear address ? [8]

(*b*) What is descriptor cache and TLB ? When they are accessed by 80386 ? What is its use ? [8]

Or

6. (*a*) How can pages be protected in 80386 microprocessor ? Explain in detail. [8]

(*b*) Write privilege checks performed by 80386 while accessing code or data with protection mechanism. List privileged and I/O sensitive instruction of 80386. [8]

SECTION II

7. (*a*) What is TSS and TSS descriptor ? Explain the function and reaction of 80386 when the task switch occurs. [10]

(*b*) What is IDT & IDTR ? What is the difference between the trap gate descriptor and the interrupt gate descriptor ? [8]

Or

8. (*a*) Compare real mode and protected mode of 80386 with respect to segmentation, interrupts processing, privilege protection and register access. [12]

(*b*) Explain the working of confirming code segment. [6]

9. (*a*) List features of 8051 and draw its internal architecture. [8]

(*b*) List interrupt sources of 8051 with vector address and priority. Draw format of IE and IP registers with their significance. [8]

Or

10. (*a*) List addressing modes of 8051 with example. [8]

(*b*) Compare with respect to use and operations carried out by 8051 : [8]

(*i*) ACALL & LCALL

(*ii*) SJMP & AJMP.

11. (*a*) Explain timer modes of 8051 with the help of TMOD and TCON registers. [8]

(*b*) List the features of PIC microcontroller and write a comment on Harward architecture of PIC microcontroller. [8]

Or

12. (*a*) State serial communication modes of 8051 with the help of SCON register and write steps for serial port programming. [8]

(*b*) List the features of Texas MSP 430. [8]