Total No. of Questions : 12]

SEAT No. :

P3644

[Total No. of Pages :3

[4758] - 81
T.E. (Computer)
MICROPROCESSORS AND MICROCONTROLLERS
(2008 Pattern) (310243)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer Question No.1 or 2, 3 or 4, 5 or 6 from Section I and Q.No. 7 or 8, 9 or 10 and 11 or 12 from Section II.***
2) ***Answers to the two sections must be written in separate answer books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data if necessary.***

SECTION - I

Q1) a) Which features make the Pentium a superscalar processor? Give details of every feature. **[6]**

b) Describe cache organization of the Pentium. **[4]**

c) Explain following pins of the Pentium. **[6]**

i) ADS #

ii) D/C#

iii) RESET

OR

Q2) a) Is the Pentium RISC or CISC or both? Justify your answer. **[4]**

b) What is branch prediction? Explain in detail. **[4]**

c) Explain Floating Point Unit of the Pentium? **[8]**

P.T.O.

Q3) a) What do you mean by bus cycle? Draw and explain burst read cycle in Pentium. **[8]**

b) Explain flag register of Pentium in detail. **[8]**

OR

Q4) a) What is bit manipulation instruction? Explain any two bit manipulation instruction. **[6]**

b) Explain addressing modes of the Pentium **[8]**

c) Describe any one instruction **[2]**

i) CMPXCHG

ii) PUSH

Q5) a) How linear address is generated in the Pentium. **[8]**

b) Describe PDE and PTE formats. **[6]**

c) Draw & explain the structure of a call gate. **[4]**

OR

Q6) a) Name protected mode registers of the Pentium. **[4]**

b) What are the selectors in the Pentium? Explain their use in segmentation. **[6]**

c) Explain rules designed to protect data or code of the Pentium. **[8]**

SECTION - II

Q7) a) What is I/O permission bit map? When it is referred? **[6]**

b) Explain task switch operation through task gate. **[6]**

c) Write any six difference between 8086 and virtual 86 mode. **[6]**

OR

Q8) a) Explain IDT in Pentium in details. How interrupt handling in protected mode is dependent on contents of IDT? **[6]**

b) Explain steps in entering Virtual mode. **[6]**

c) Explain nested task in Pentium. **[6]**

Q9) a) Draw and Explain internal RAM organization of 8051. **[12]**

b) Explain the function of following pins **[4]**

i) T1

ii) T0

OR

Q10)a) Explain port 0 to port 3 of 8051. **[8]**

b) Explain following 8051 instructions **[8]**

i) POP

ii) ANL

iii) MUL AB

iv) LCALL

Q11)a) Write features of 8096 microcontroller. **[4]**

b) Explain addressing modes of 8051 microcontroller. Explain with suitable example. **[8]**

c) Explain any two modes of timer operation in 8051. **[4]**

OR

Q12)a) What are the different sources of interrupts in 8051? Explain interrupt handling mechanism in 8051. **[8]**

b) Explain IE register of 8051 microcontroller. **[4]**

c) Explain PCON of serial port of 8051 microcontroller. **[4]**

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