T.E. (Computer Engineering)
DIGITAL SIGNAL PROCESSING APPLICATIONS
(2012 Pattern) (310253) (Semester - II) (End - Sem.)

Time : 3Hours]   *[Max. Marks : 70*

Instructions to the candidates:

1) Attempt Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10.

2) Neat diagrams must be drawn wherever necessary.

3) Assume suitable data if necessary.

Q1) a) Define two standard signals $u(n)$ and $\delta(n)$. Show that $u(n) = \sum_{k=0}^{\infty} \delta(n-k)$

by means of convolution operation. **[5]**

   b) State Periodicity and Symmetry property of DFT. How can we compute N point Circular Convolution using DFT and IDFT? **[5]**

OR

Q2) a) Perform following circular shifting operations on a given DT signal **[5]**

$x(n) = \{1, 2, 3, 4\}$ with N = 5 and N = 6

   i) $x((n-3))N$

   ii) $x((n+2))N$

   b) Discuss the form of an Nth order difference equation used to describe a DT system. How can it be expressed as an FIR and IIR system? **[5]**

Q3) a) Derive the first stage of DIT FFT algorithm. How the computational efficiency is improved in FFT algorithm? **[5]**

   b) Obtain the Z Transform of sequence $x(n) = a^n u(-n-1)$ and sketch the ROC. **[5]**

OR

Q4) a) How can we compute Linear Convolution using N point Circular Convolution? **[5]**

   b) Define system function H(Z). Obtain it from the Nth order difference equation and express it for All Pole and All Zero System. **[5]**

Q5) a) What are filter structures? Explain how the Direct and Cascade form of FIR filters are obtained and realized from the system function H(Z). **[9]**

b) A DT System described by means of system function H(Z) is given by- **[9]**

$$H(Z)=3+\frac{4Z}{Z-1/2}-\frac{2}{Z-1/4}$$

Obtain and Draw Direct Form - I and Direct Form - II IIR filter structure.

OR

Q6) a) Obtain and realize Linear Phase FIR filter structure for a DT system.**[9]**

$$H(Z)=\left(1+\frac{1}{2}Z^{-1}+Z^{-2}\right)\left(1+\frac{1}{4}Z^{-1}+Z^{-2}\right)$$

What are the advantages of this filter structure?

b) Derive the Direct Form - II IIR filter structure from system function H(Z) and represent it using multipliers, adders and delay elements. **[9]**

Q7) a) Draw the block diagram of basic DSP processor. What are the common features of DSP processor? **[8]**

b) Explain how SHARC DSP processor supports the multiprocessing capabilities. Give details about different types of ports used for multiprocessing. **[8]**

OR

Q8) a) What is OMAP? Explain the Hardware architecture of OMAP in brief.**[8]**

b) Compare between Harvard and Super Harvard Architecture of DSP Processor. List the number of DAGs and supporting memory pointer registers of SHARC DSP Processor. **[8]**

Q9) a) Explain the following terms associated with audio processing: **[8]**

   i) Timbre

   ii) Loudness

   iii) Pitch

   b) What is image enhancement in digital image processing? Explain any two gray level transforms used for image enhancement. **[8]**

<div align="center">OR</div>

*Q10)*a) What do you mean by Speech Synthesis and Recognition? Draw and explain Human Speech Model in brief. **[8]**

   b) Explain the operation of CCD (Charge Coupled Device) used in electronic cameras. **[8]**

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