Total No. of Questions : 12]

SEAT No. :

P3379

[Total No. of Pages : 3

[4959]-118
B.E. (Electronics)
a-ADVANCED COMPUTER ARCHITECTURE
(Semester - I) (2008 Pattern) (Elective - II) (404205)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answer three questions from Section - I and 3 questions from Section -II.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagram must be drawn whenever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data if necessary.***

SECTION - I

Q1) a) Discuss in detail the application of parallel processing in **[12]**

i) Predictive modelling and simulation.

ii) Engineering design and automation.

b) Discuss and explain instruction level parallelism and Thread level parallelism. **[6]**

OR

Q2) a) Discuss Flynn's & Handler's classification of parallel computer in detail. **[12]**

b) Explain the Amdahl's law for speedup performance. **[6]**

Q3) a) Explain various types of data hazards observed in pipeline processor. How those hazards could be detected and resolved. **[8]**

b) Compare between: **[8]**

i) Static and dynamic pipeline

ii) Unifunctional and multifunctional pipeline.

OR

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Q4) a) Explain the Internal Forwarding Techniques. **[6]**

b) Consider the following pipeline reservation table

clock cycles → / States ↓	1	2	3	4	5	6	7
S1	X		X				X
S2				X		X	
S3			X		X		

[10]

i) Determine latencies in the forbidden list F and collision vector C.

ii) Draw the state transition diagram.

iii) List all simple cycles and greedy cycles.

iv) For a pipeline clock period τ= 20ns. Determine maximum throughput of the pipeline.

Q5) a) What are vector processors? Discuss two different architectural configurations of vector processor. **[12]**

b) Explain pipeline chaining. **[4]**

OR

Q6) a) State the characteristics of CRAY - 1 computer system. Draw and explain the computation section of CRAY - 1 vector processor. **[12]**

b) Explain any two types of vector instructions. **[4]**

SECTION - II

Q7) a) Explain matrix multiplication on SIMD architecture. **[10]**

b) Explain the cube interconnection network and hypercube interconnection network. **[8]**

OR

Q8) a) Explain the algorithm to compute fast Fourier Transform for SIMD architecture. **[10]**

b) Explain static and dynamic network topologies used in interconnection networks with proper examples. **[8]**

Q9) a) Explain cache coherency and bus snooping. **[8]**

b) Explain loosely and tightly coupled multiprocessor system with example. **[8]**

OR

Q10)a) Explain in detail chip multiprocessing. **[8]**

b) Give a typical architecture for MPP. Explain in detail. **[8]**

Q11)a) Discuss in brief latency hiding techniques. **[8]**

b) Explain Data parallel programming. **[8]**

OR

Q12)a) Write short note on **[8]**

i) Synchronous message passing

ii) Asynchronous message passing

b) Explain use of following primitives w.r.t. parallel programming. **[8]**

i) Send ( );

ii) Receive ( );

iii) Fork ( );

iv) Join ( );