Total No. of Questions :12]

SEAT No. :

P3375

[Total No. of Pages :3

[4959]-113
B.E. (Electronics)
VLSI Design
(2008 Course) (Semester -I) (404202)

Time : 3 Hours *[Max. Marks :100]*

Instructions to candidates:

1) ***Answer 03 questions from section I and 03 questions from secetion II.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data if necessary.***
6) ***Use of logarithmic tables slide rule, mollier charts, electronic pocket calculator and steam tables is allowed.***

SECTION -I

Q1) a) Explain CMOS inverter and also show the voltage transfer curve with all the region of operation of NMOS and PMOS. **[7]**

b) Explain the following. **[9]**

i) Hot electron effect.

ii) Body effect.

iii) Velocity saturation.

OR

Q2) a) Draw 8:1 MUX using transmission gate and compare the same with conventional diagram of MUX. **[8]**

b) Differentiate between Static and dynamic power dissipation considering any one digital circuit. **[8]**

Q3) a) Enlist all the memories used in CMOS technology. **[8]**

b) Differentiate between SRAM and DRAM and show how both memories are different from each other. **[8]**

OR

P.T.O.

Q4) a) With the help of diagram explain single bit SRAM. **[8]**

b) Explain the role of memories in PLDs. **[8]**

Q5) a) Explain all the modeling styles used in VHDL design considering the example of 4:1 MUX. **[9]**

b) Differentiate the following. **[9]**

i) Synthesizable and non synthesizable test benches.

ii) Function and procedure.

iii) Moore and Mealey machine.

OR

Q6) a) Write a VHDL code for Moore machine and Mealey machine and Comment on the result which detects the sequence 1010. **[12]**

b) Define metastability. How it can be reduced? **[6]**

SECTION -II

Q7) a) Explain the role of PLDs in DSP processor. **[8]**

b) Draw the block diagram of FPGA and explain CLBs in detail. **[8]**

OR

Q8) a) Enlist and explain all the types of PLDs. **[8]**

b) With the help of block diagram explain CPLD and also explain how it is different from other PLDs. **[8]**

Q9) a) Define controllability and predictability. How these two factors are contributing in testability. **[8]**

b) Explain stuck at 1 and stuck at 0 faults. **[8]**

OR

Q10)a) Explain the architecture of JTAG showing all the required signals. **[8]**

b) Differentiate partial and full scanning giving suitable example. **[8]**

Q11)a) Enlist all the signal integrity issues and also give the methods to avoid the problem of EMI. **[9]**

b) What are the different methods of clock distribution technique. **[9]**

OR

Q12)Explain the following (Any three). **[18]**

a) Clock skew.

b) Clock jitter.

c) EMC techniques.

d) H- tree.

e) Power optimization techniques.