Total No. of Questions : 10]

SEAT No. :

P3622

[Total No. of Pages : 2

[4959] - 1108
B.E. (Electronics)
DSP Processors
(Semester - I) (Elective - II) (2012 Course)

Time :2.½ Hours] *[Max. Marks :70*

Instructions to the candidates:-

1) ***Answer Q. 1 or Q. 2, Q. 3 or Q. 4, Q. 5 or Q. 6, Q. 7 or Q. 8, Q.9orQ.10.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figure to the right side indicates full marks.***
4) ***Assume suitable data if necessary.***
5) ***Use of logarithmic tables slide rule mollier charts, electronic pocket calculator and steam tables is allowed.***

Q1) a) Explain the various sources of error in DSP implementations. **[6]**

b) Discuss any four common architectural features implemented in Digital Signal Processors. **[4]**

OR

Q2) a) Discuss the important issues considered in implementing a DSP system **[6]**

b) Explain briefly selection criteria of DSP processors. **[4]**

Q3) a) What is the need of Barrel shifter in DSP architecture? Explain in detail. **[6]**

b) Explain the dynamic range and precision in context with DSP. **[4]**

OR

Q4) a) What is the use of pipelining in DSP? Explain in detail. **[6]**

b) What is meant by overflow in an arithmetic computation? How is an overflow condition detected? **[4]**

Q5) a) Explain the implementation of FIR filter in DSP system. **[8]**

b) Explain the Q-notations used in DSP algorithm implementation? State the difference between floating point and fixed point processing. Suggest suitable application for each fixed and floating point processing. **[9]**

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OR

Q6) a) Explain the 2-D signal processing operation used in DSP implementations. **[8]**

b) What is multirate digital signal processing? Suggest suitable application of the same. Explain interpolation and decimation filters briefly. **[9]**

Q7) a) Explain the following in context with FFT algorithm: **[8]**

i) Need of zero padding

ii) Overflow and Scaling

iii) Bit reversed index generation

b) Explain the implementation 8 point DIT FFT algorithm using signal flow graph and number of arithmetical computation involved. **[9]**

OR

Q8) a) What is difference between Fourier Series and Fourier Transform? Explain the computation of Signal spectrum using fourier transform. How will you increase the resolution of the spectrum? **[8]**

b) A time domain sequence of 15 elements is to be convolved with another time domain sequence of 10 elements using DFT – IDFT method. A radix 2 DIT FFT algorithm is used. Determine the total number of complex multiplications needed to implement the convolution. Assume that each butterfly computation requires one complex multiplication. **[9]**

Q9) a) What is DMA? How does DMA help in increasing the processing speed of a DSP Processor? **[8]**

b) What is the Hardware interrupt and Software Interrupt? Classify interrupts of TMS320C5416 processor **[8]**

OR

Q10) a) What is the role of CODEC in DSP. Explain McBSP in context with DSP processor? **[8]**

b) Explain the Memory Interfacing with suitable diagram? How many address lines are required to access all locations of an 16K × 16 SRAM. **[8]**

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