Total No. of Questions : 10]

SEAT No. :

P4943

[Total No. of Pages :2

[4959]-1120
B.E. (Electronics)
C : SYSTEMS ON CHIP
(2012 Pattern) (Semester - II)

Time : 2.30 Hours] *[Maximum Marks : 70*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8, Q.9 or Q.10.***
2) ***Draw neat diagrams.***
3) ***Assume suitable data, if necessary.***

Q1) a) How to avoid data loss using FIFO? What are its limitations? **[6]**

b) Which factors acted as barriers to the use of the Microsystems technology? **[4]**

OR

Q2) a) Explain in the TRIMEDIA processor specifications and performance metrics. **[6]**

b) Why latches should be avoided in design? What is good practice to avoid latches? **[4]**

Q3) a) What do you mean by loop folding? Explain it in context with constraint propagation and interval analysis. **[6]**

b) Why at RTL stage, it is very difficult to know the actual delays? **[4]**

OR

Q4) a) Explain with example constraint propagation. **[6]**

b) What is the reason of this pre and post synthesis simulation mismatch? **[4]**

P.T.O.

Q5) a) Which factors plays important role while developing mathematical model for analysis of MEMS? **[8]**

b) Explain Structured Design Methods for MEMS? **[8]**

OR

Q6) a) What do you mean by scaling in electromagnetic force? Justify: electromagnetic force is $F \alpha l^4$. **[8]**

b) Compare GaAs Vs Silicon. **[8]**

Q7) a) Explain pros and cons of behavioral synthesis. **[8]**

b) Explain abstraction levels in contact to synthesis tool. **[8]**

OR

Q8) a) Compare of bulk-and surface-micromachining processes for MEMS fabrication. **[8]**

b) What are wet-etch selection and development principles? **[8]**

Q9) a) Explain the terms- **[9]**

i) Defects and fault method

ii) Fault simulation

b) What are the issues in testing of core based systems on chip? **[9]**

OR

Q10)a) Explain features of co-design tool with an example. **[9]**

b) What are the requirements of packaging? Which materials are used at this stage? **[9]**

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