Total No. of Questions : 10]

SEAT No. :

P3616

[Total No. of Pages : 2

[4959] - 1101
B.E. (Electronics Engineering)
VLSI DESIGN (Theory)
(2012 Course) (Semester - I)

Time :2½ Hours] *[Max. Marks :70*

Instructions to the candidates:-

1) ***Neat diagrams must be drawn wherever necessary.***
2) ***Figures to the right indicate full marks.***
3) ***Use of logarithmic tables slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.***
4) ***Assume suitable data, if necessary.***

Q1) a) Prove that to achieve completely symmetric input output characteristics for a CMOS inverter, the design requires to have $(W/L)_P = 2.5(W/L)_N$ Assume that the gate oxide thickness t_{ox}, and hence the gate oxide capacitance C_{ox} have the same value for both NMOS and PMOS transistors. **[6]**

b) Write short notes on Channel length Modulation. **[4]**

OR

Q2) a) Draw and Explain I_{ds} - V_{ds} characteristics of NMOS. **[5]**

b) Explain noise margin. Give its expressions. **[5]**

Q3) a) Write VHDL code for 4 bit up - down counter. **[5]**

b) Draw the block diagram and explain the architecture of FPGA. **[5]**

OR

Q4) a) Explain data types in VHDL with suitable examples. **[5]**

b) What is metastability? How can it be removed? **[5]**

P.T.O.

Q5) a) Draw the schematic of DRAM cell with necessary peripherals and explain read write cycles with the help of timing diagram. **[8]**

b) Explain memory organization in details. **[8]**

OR

Q6) a) Draw and explain the schematic of SRAM cell with necessary peripherals. **[8]**

b) Write short notes on **[8]**

i) Refresh circuit

ii) Sense amplifier

Q7) a) What are the challenges in routing? Explain switchbox routing. **[8]**

b) Explain floor planning, its purpose and the rules. **[8]**

OR

Q8) a) What is Global Routing. Explain Maze and line probe routing. Algorithms in details. **[8]**

b) Explain Power distribution and power optimization in details. **[8]**

Q9) a) What are stuckopen, stuck short faults? Also explain stuck at 1 and stuck at 0 faults with an example. **[9]**

b) What is built in sefl test? Explain BIST for RAM. **[9]**

OR

Q10) a) What is Test access port? Explain TAP Controller with the help of state machine. **[8]**

b) With reference to BIST, explain the following terms **[6]**

- LFSR
- Scan chain for flip flop

c) Explain **[4]**

- Controllability
- Observability

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