

Total No. of Questions : 06]

SEAT No. :

P3790

[Total No. of Pages : 3

[4960] - 1308

M.E. (Computer)

**Advanced Computer Architecture
(2013 Pattern)**

Time : 3 Hours]

[Max. Marks : 50

Instructions to the candidates:

- 1) *All questions are compulsory.*
- 2) *Neat diagram must be drawn wherever necessary.*
- 3) *Figures to the right side indicate full marks.*
- 4) *Assume suitable data, if necessary.*

- Q1)** a) What is the significance of PRAM models? Describe the four variants of PRAM model and compare it with parallel computer architectures [5]
- b) Discuss in brief the fine grain and coarse grain scheduling w.r.t. multiprocessor scheduling. [4]

OR

- a) How data hazards are classified? State the Bernstein's conditions used for the detection of parallelism. [5]
- b) Compare between static and dynamic Interconnection Networks used in array processor systems [4]

- Q2)** a) What is the significance of Scalability? Describe the term Speedup and Efficiency w.r.t. scalability [4]
- b) Derive the Amdahl's law for speedup performance. Comment on the major observations and conclusions drawn w.r.t. the speedup obtained. [4]

OR

P.T.O.

- a) Compare SIMD architecture with MIMD in terms of processing nodes, Interconnection Networks, parallelism and the performance in brief. [4]
- b) Compare S/w parallelism with H/w parallelism. State few methods/techniques implemented by means of S/w and H/w architecture in parallel computer system to achieve the S/w and H/w parallelism [4]

- Q3)**
- a) Define the term Instruction issue latency. How it affects on the performance of pipelined processor? What is the use of Reservation Table? [4]
 - b) With example illustrate the design of an arithmetic pipeline [4]

OR

- a) Discuss in brief the following important properties related to the information stored in Memory Hierarchy: [4]
 - i) Inclusion
 - ii) Coherence
- b) Explain in brief any two dynamic instruction scheduling schemes w.r.t. an instruction pipeline. [4]

- Q4)**
- a) What are multi-threaded architectures? Discuss the various performance parameters of multi-threaded processor architectures. [4]
 - b) What is cache coherency? How it is insured in multiprocessor systems? Compare between Write Invalidate and Write Update protocols. [4]

OR

- a) What is data parallel programming? Explain the terms SPMD and MPMD w.r.t. parallel programming [4]
- b) How vector looping is implemented in Cray architecture? Illustrate with example and state its advantages. [4]

- Q5)** a) With example explain shared memory parallel programming. [4]
- b) Explain the features and standard constructs used in High Performance Fortran (HPF) or Fortran-90 for parallel programming [4]

OR

- a) Discuss the important features of MPI and PVM message passing libraries. How it helps in parallel programming? [4]
- b) Comment on thread and process level parallelism with support of an OS for the parallel program execution [4]

- Q6)** a) How Cloud computing differs from Cluster Computing? State with example SaaS, PaaS and IaaS Services offered by Cloud. [5]
- b) How Neural Networks can be used for distributed parallel computing? Discuss in brief. [4]

OR

- a) Explain the following terms w.r.t. Grid computing - [5]
- i) Middleware
 - ii) OGSA
 - iii) OGSI
- b) Discuss the features of GPU parallel architecture [4]

