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Seat No.	
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[4957]-1073

S.E. (Computer) (First Semester) EXAMINATION, 2016
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

- N.B. :—** (i) Attempt Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,
Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.
(ii) Neat diagrams must be drawn wherever necessary.
(iii) Figures to the right indicate full marks.
(iv) Assume suitable data, if necessary.

1. (a) Minimize the following function using k -Map and realize using logic gates : [4]
 $F(A, B, C, D) = \sum m(0, 2, 5, 8, 11, 15) + d(1, 7, 14)$.
(b) Convert the following : [2]
 $(175)_{10} = (?)_8$.
(c) List the differences between CMOS and TTL. [6]

Or

2. (a) Represent the following signed number in 2's complement method : [2]
(i) +18
(ii) -18.
(b) Define the following terms and mention its standard values for TTL family : [6]
(i) Voltage parameters
(ii) Power dissipation
(iii) Fan out.

P.T.O.

(c) Do the following conversions : [4]

(i) $(582C)_{16} \rightarrow (?)_2$

(ii) $(417.125)_{10} \rightarrow (?)_2$.

3. (a) Explain rules for BCD addition with suitable example and design a single digit BCD adder using IC 7483. [6]

(b) Design a MOD-6 synchronous counter using J-K flip-flops [6]

Or

4. (a) Design a 4 bit BCD to Excess-3 code convertor circuit using minimum number of logic gates. [6]

(b) Design a sequence generator using J-K FF. Sequence is : [6]

$1 \rightarrow 3 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 1.$

5. (a) State and explain basic components of ASM chart. Also explain the salient features of ASM chart. [7]

(b) Write a VHDL code for 8 : 1 multiplexer using behavioural modeling. [6]

Or

6. (a) Draw ASM chart for the following state machine :

A two bit up counter with output 'BA' and enable signal 'X' is to be designed. If 'X' = 0, counter changes the state as '00-01-11-00'. If 'X' = 1, counter should remain in present state. Design the circuit using multiplexer controller method. [8]

(b) State differences between concurrent and sequential statements of VHDL. [5]

7. (a) Draw and explain the basic architecture of FPGA. [6]
(b) What are the different types of PLDs ? Design 3 : 8 decoder using PLD. [7]

Or

8. (a) Compare PROM, PLA and PAL. [6]
(b) A combinational circuit is defined by the function :
$$F_1(A,B,C) = \Sigma m(0, 1, 2, 4)$$
$$F_2(A,B,C) = \Sigma m(1, 3, 5, 6)$$
Implement this circuit with PLA. [7]