Seat	
No.	

[4957]-1075

S.E. (Computer Engineering) (First Semester)

EXAMINATION, 2016

MICROPROCESSOR ARCHITECTURE

(2012 **PATTERN**)

Time: Two Hours

Maximum Marks: 50

- N.B. :— (i) Answer any four questions, Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.
 - (ii) Neat diagrams must be drawn wherever necessary.
 - (iii) Figures to the right indicate full marks.
- 1. (a) Explain all control registers (CRO to CR3) of 80386DX microprocessor in detail. [6]
 - (b) What is maximum memory addressing capability of 8086 processor? In what way 80386 system is different from 8086 memory organization?
 - (c) Explain the significance of the following signals with reference to 80386 microprocessor: [2]
 - (i) BE# to BE#
 - (ii) READY.

Or

2. (a) What is MSW (Machine status word) in 80386DX microprocessor? Draw its format and explain. [6]

P.T.O.

	(<i>b</i>)	Explain various memory /10 interface signals of 80386DX
		processor [4]
	(c)	Enlist the features of 8086 microprocessor [2]
3.	(a)	What is Virtual 86 mode. Explain in detail. [5]
	(<i>b</i>)	With the help of suitable timing diagram explain the pipelined
		bus cycles in 80386 processor. [4]
	(c)	Explain the following instructions with examples: [3]
		(i) BSR
		(ii) CLTS
		(iii) DAA.
		Or
4.	(a)	Explain in detail how to switch from real mode to V86
		mode. [6]
	(<i>b</i>)	Compare and contrast procedure and macro. [4]
	(c)	Differentiate between DIV and IDIV instruction. [2]
5.	(a)	Explain common configurations that support multiprocessing in
		detail. [6]
	(<i>b</i>)	Explain in detail different points to be considered to take full
		advantage of multicore platform. [4]
	(c)	What are the differences between multi-processing and multi-
	\ -/	tasking. [3]
		Or
6.	(a)	Write a short note on multicore design and implemen-
	, ,	tation. [6]
	(<i>b</i>)	Differentiate between multiprogramming and multiprocessing.
	(0)	[4]
		L *1

	(c)	List the advantages and disadvantages of Virtualiza	tion
		Technology.	[3]
7.	(a)	Explain any six 64-bit mode instruction.	[6]
	<i>(b)</i>	Write a short note intel Hyper Threading Technology	[4]
	(c)	List the features of SSE2.	[3]
		Or	
8.	(a)	Explain with functional block diagram of Intel microarchitec	
		code name Nehalem.	[6]
	(<i>b</i>)	What is single instruction multiple data model for par-	allel
		programming.	[4]
	(c)	Briefly explain the compatibility mode and 64-bit mode of	f IA
		64 architecture.	[3]