Total No. of Questions—**8**] [Total No. of Printed Pages—**4**

Seat No.	

[4957]-1083

S.E. (Information Technology) (First Semester)

EXAMINATION, 2016

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**, Q. No. **7** *or* Q. No. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Assume suitable data, if necessary.

1. (*a*) Draw and explain 2 input TTLNAND gate. [6]

(*b*) Design using single 4 : 1 multiplexer and logic gates : [6]

$F(A, B, C, D) = \Sigma m(0, 2, 5, 8, 10, 15)$.

Or

2. (*a*) Convert the Decimal number 27 into : [6]

(*i*) Binary

(*ii*) Excess-3

(*iii*) Gray

(*iv*) HEX.

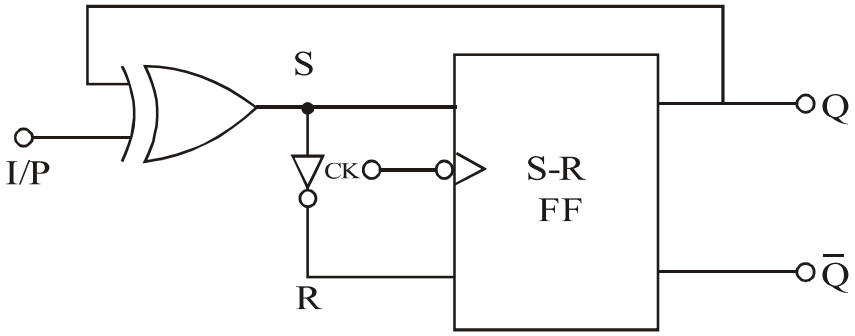
P.T.O.

(*b*) Design Multiple output functions using IC 74138 and Logic Gates : [6]

$$F_1(A, B, C) = \pi M(0, 1, 3, 7) \text{ and}$$

$$F_2(A, B, C) = \pi M(2, 3, 7).$$

3. (*a*) Write the Excitation Table of S-R flip-flop. Prepare the Truth Table for the following circuit and Determine the type of flip-flop. [6]



(*b*) Draw 4-bit Twisted Ring Counter using D Flip-Flop. Consider initially all flip-flops are cleared. What will be the output after 5th Clock Pulse and Prove that the Modulus of this Twisted Ring Counter is 8. [6]

Or

4. (*a*) Design T flip-flop using JK flip-flop. [4]

(*b*) Draw an ASM chart for the 2-bit Up/Down counter having mode controlled input 'M'. if M = 0; Counter holds the present state and if M = 1; Counter goes to the next state. [4]

(*c*) Design and draw Logic Diagram of MOD-99 Counter using IC 7490. [4]

5. (*a*) Draw and explain the architecture of FPGA. [6]

(*b*) A combinational Circuit is defined by the following functions :

$$F_1 = \Sigma m(3, 5, 7)$$

$$F_2 = \Sigma m(4, 5, 7) \text{ and}$$

$$F_3 = \Sigma m(3, 4, 5).$$

Design the circuit with a PLA having 3 intputs, 3 product terms and 3 outputs. [7]

Or

6. (*a*) Give the comparison with PLA and PAL with respect to architecture flexibility and advantages and disadvantages. [6]

(*b*) Design the following functions using PLA with 4 inputs, 6 product team and 3 outputs : [7]

$$X = ABC + B'D' + AB'D + C'D'$$

$$Y = BC + D'$$

$$Z = CD + B'D' + A'BC.$$

7. (*a*) Explain Entity and Architecture in VHDL with syntax and example. [6]

(*b*) Explain data objects in VHDL : [7]

Signal, Variable and Constants.

Or

8. (*a*) What is VHDL ? What are the advantages of VHDL ? What are the features of VHDL ? [6]

(*b*) What is the difference between sequential execution and concurrent execution of VHDL statement ? Explain with the help of suitable example. [7]