Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[5057]-257

S.E. (Comp. Engg.) (Second Semester) EXAMINATION, 2016

MICROPROCESSOR AND INTERFACING TECHNIQUES

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. Nos. **1** *or* **2**, Q. Nos. **3** *or* **4**, Q. Nos. **5** *or* **6**, Q. Nos. **7** *or* **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

1. (*a*) Compare 8086, 80386 and i7 processor on the basis of architectural features. [4]

(*b*) List the differneces between .com and .exe. [4]

(*c*) List and explain 80386 bus cycles required to fetch and execute the instruction IN AX, 3C H. [4]

Or

2. (*a*) Explain base addressing mode. Indicate your answer with examples of instructions using these addressing mode with respect to 80386. [4]

(*b*) Draw and explain IVT. [4]

P.T.O.

(*c*) Write initialization instructions for 8259 to meet the following specifications : [4]

(*i*) Interrupt type 64

(*ii*) Level triggered, Single, ICW4 needed.

3. (*a*) Explain the difference between synchronous and asynchronous serial communication. [3]

(*b*) Explain in brief port structure of 8255 PPI. [5]

(*c*) What are different sources of errors in DAC ? [4]

Or

4. (*a*) Prepare a control word to initialize 8279 in the following given keyboard/display mode : [4]

(*i*) 16, 8-bit character left entry

(*ii*) Decoded scan n-key rollover.

(*b*) Give the control word format for 8253/8254. [4]

(*c*) Explain with a neat diagram sequence of DMA operation. [4]

5. (*a*) Draw and explain maximum mode configuration of 8086. [7]

(*b*) Write notes on the following supporting chips : [6]

(*i*) 8284

(*ii*) 8286

(*iii*) 8288.

Or

6. (*a*) Draw and discuss the interface between 8086 and 8087. [7]

(*b*) Explain the data format for 8087 NDP in brief. [6]

7. (*a*) Draw and explain block diagram of Intel Core i5. [7]

(*b*) Explain the features of 82801 IJR I/O Controller Hub. [6]

Or

8. (*a*) Draw and explain block diagram of x58 chip set. [7]

(*b*) Write a short note on Serial ATA controller and QIP Technology. [6]