Total No. of Questions—**8**] [Total No. of Printed Pages—**3**

Seat No.	

[5057]-262

S.E. (I.T.) (I Sem.) EXAMINATION, 2016

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Use of calculator is not allowed.

(*iv*) Assume suitable data, if necessary.

1. (*a*) Which parameters are significant while interfacing TTL and CMOS ? Draw and explain the interfacing of CMOS and TTL. [6]

(*b*) What do you mean by half-adder and full-adder ? How will you implement full-adder using half-adder ? Explain with circuit diagram. [6]

Or

2. (*a*) Convert the following hexadecimal numbers into their equivalent Binary, Octal and decimal numbers : [6]

(*i*) $(9CFD)_{Hex}$

(*ii*) $(0FDE)_{Hex}$.

P.T.O.

(*b*) Implement the following function using 4 : 1 multiplexer. Show step-by-step implementation : [6]

$F(A, B, C, D) = \Sigma m(1, 2, 7, 8, 10, 12, 15)$.

3. (*a*) Explain the difference between asynchronous and synchronous counter and convert S-R flip-flop into D-FF. Show the design steps. [6]

(*b*) Draw ASM chart for the following state machine : [7]

A two bit UP counter with enable signal "M" is to be designed. If 'M" = 0, counter changes the state as 0-1-2-3. If 'M' = 1, counter should remain in present state. Draw state table for the circuit and design the circuit to generate the output using MUX controller method. [7]

Or

4. (*a*) Design and draw logic diagram of MOD-98 counter using IC 7490. [6]

(*b*) Design sequence detector to detect the sequence ..... 1011 ..... using JK flip-flop. [7]

5. (*a*) Explain the difference between CPLDs and FPGAs. [6]

(*b*) Design full subtractor with suitable PLA. [6]

Or

6. (*a*) Design 3-bit binary to Gray code convertor and implement using suitable PLA. [6]

(*b*) Explain difference between PAL and PLA. [6]

7. (*a*) What is VHDL ? Write features of VHDL. Explain the structure of VHDL module. [6]

(*b*) Explain process statement in behaviour model of VHDL with respect to syntax, sensitivity list, declarative part and statement part with *one* example. [7]

Or

8. (*a*) Explain the different VHDL Modeling styles — Data flow, Behavioral and structural. [6]

(*b*) Define entity declaration for Ex-OR gate. Also write architecture of Ex-OR gate in structural and data flow modeling style. [7]