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Seat No.	
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**[5057]-2055**

**S.E. (Computer) (First Semester) EXAMINATION, 2016**

**COMPUTER ORGANIZATION AND ARCHITECTURE**

**(2015 Pattern)**

**Time : Two Hours**

**Maximum Marks : 50**

**N.B. :—** (i) Neat diagrams must be drawn wherever necessary.

(ii) Figures to the right indicate full marks.

(iii) Use of calculator is allowed.

(iv) Assume suitable data, if necessary.

1. (a) Show the general structure of IAS computer and explain in detail. [6]

(b) Explain following cache mapping techniques along with their merits and demerits : [6]

(i) Direct

(ii) Set associative.

*Or*

2. (a) Perform Division of following numbers using restoring Division Algorithm : [6]

Dividend = 1011

Divisor = 0011.

P.T.O.

- (b) What is Cache coherence ? What are the solutions to cache coherence problem in single CPU system. [6]
3. (a) What are the evolutionary steps of I/O channel ? Explain types of I/O channel ? [6]
- (b) Explain the following addressing modes with *one* example each :
- (i) Immediate
  - (ii) Register Indirect
  - (iii) Direct.

*Or*

4. (a) Differentiate between programmed I/O and interrupt driven I/O. [6]
- (b) What is displacement addressing ? Explain its types with calculation of effective address. [6]
5. (a) What are various hazards in instruction pipelining ? Explain with example. [7]
- (b) What is register organization ? What are different types of registers ? Explain in detail. [6]

*Or*

6. (a) Explain the instruction cycle in detail. [6]
- (b) List and explain various ways in which an instruction pipeline can deal with conditional branch instructions. [7]

7. (a) Compare horizontal and vertical microinstruction format. [6]  
(b) Write a control sequence for the following instruction for single bus organization : SUB (R3), R1. [7]

*Or*

8. (a) Compare Hardwired control over micro-programmed control. [6]  
(b) Explain in detail micro instruction sequencing organization. [7]